Supporting Information: High-Current Density $SmTiO_3/SrTiO_3$ Field-effect Transistors

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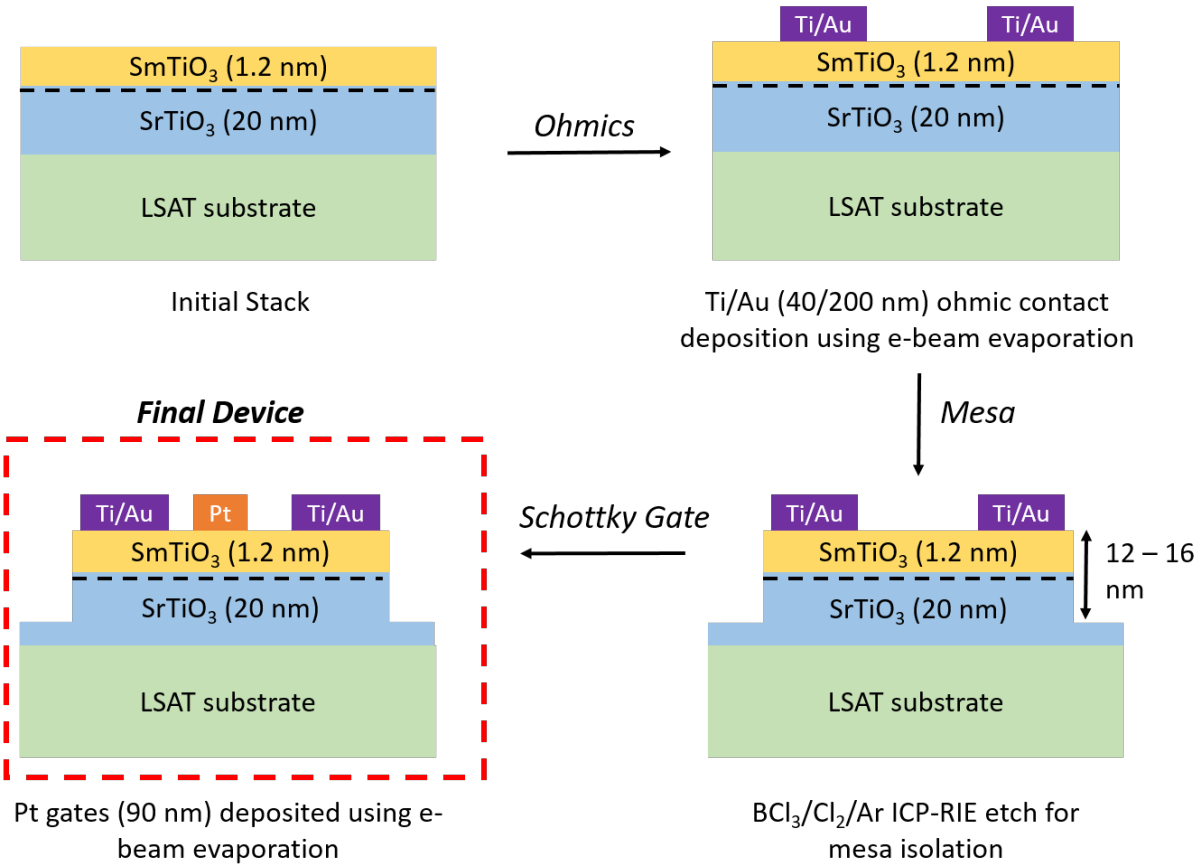

Figure S1*: Schematic process flow for device fabrication used in this study. All steps were carried out using i-line stepper lithography.*

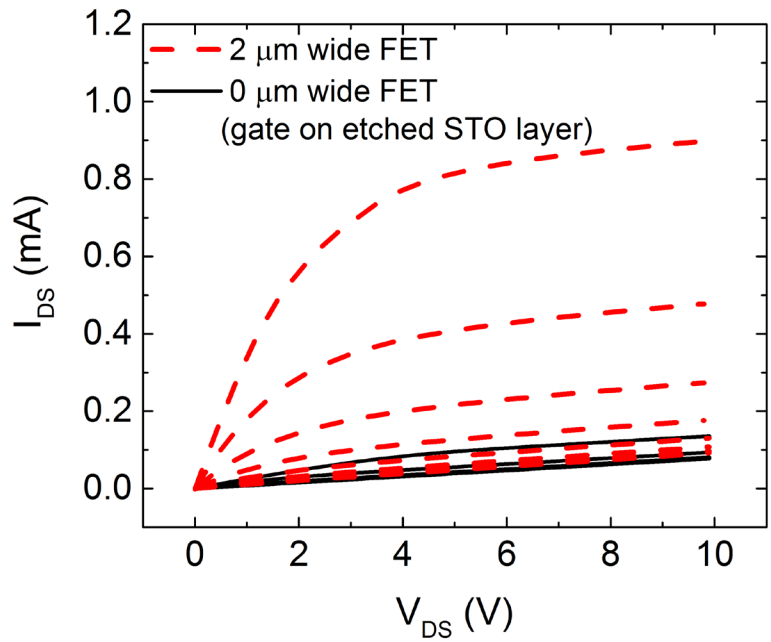

Figure S2*: Measured FET output characteristics (un-normalized) for a 2 μm wide SmTO/STO transistor as compared to a device with no constriction i.e., gate directly on the STO layer (100 μm wide STO transistor). The "leakage" currents due to the 100 μm wide STO layers are quite small (<15%) as compared to those observed for the 2 μm wide SmTO/STO channels.*

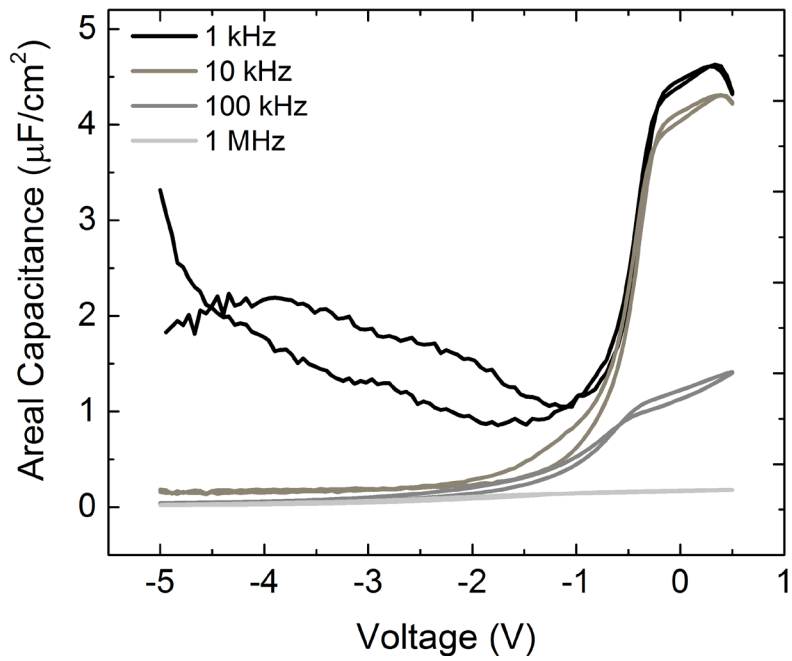

Figure S3*: Measured capacitances for frequencies of 1 kHz, 10 kHz, 100 kHz and 1 MHz at room temperature on circular capacitor structures (200 μm diameter) on the SmTO/STO stacks. Accumulation capacitance is dominated by quantum capacitance of the confined 2D electrons and dispersion is observed in both accumulation and depletion regions.*

Material Property	*$SmTiO_3$*	*$SrTiO_3$*
Dielectric Constant (ε_r)	30	200
Band gap (eV)	4.85	3.27
Electron affinity (eV)	2.35	3.9
Polarization (C/m^2)	0.16	0

***Table S1**: Material properties of $SmTiO_3$ and $SrTiO_3$ from Ref.[1] used for generating the band diagram shown in the main text. A spontaneous polarization of 0.16 C/m^2 was used for $SmTiO_3$ in order to obtain a channel electron density of 10^{14} cm^{-2}.*

Origin of the parasitic series resistance –Apart from the channel resistance, the series resistance contributions are two-fold – contact and access resistances. This is shown in the schematic below.

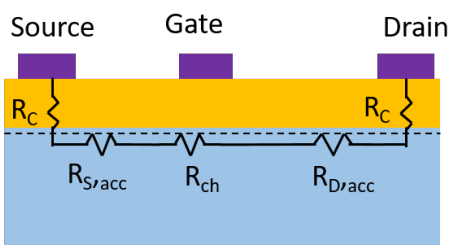

***Figure S4**: Schematic of device resistances for the transistor structure in this study.*

The total resistance of the device is $R_{tot} = 2R_C+R_{S,acc}+R_{D,acc}+R_{ch}$. Given the high contact resistances and the inherent sheet resistivity of the 2DEG, these contact and sheet resistance contributions are fairly high for the SmTO/STO system in this case. For instance, Figure S5 shows a plot of resistance vs pad spacing for 100 µm wide TLM pads to quantify the contact resistance.

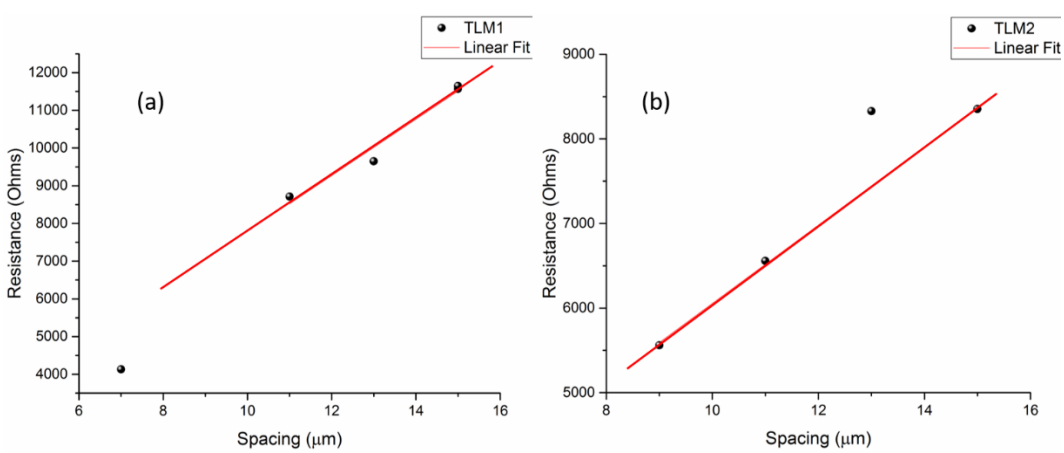

***Figure S5**: Measured resistance vs spacing for two sets of 100 μm wide TLM pads on the SmTO/STO 2DEGs in this study.*

It is important to note the spread in the measured resistances, both for various TLM spacings as well as across the two different sets of TLMs which are indicative of the fabrication challenges in making good quality low-resistance ohmic contacts to $SrTiO_3$ based 2DEGs.

Furthermore, the contact resistance from the best-case fit for the two cases shown above is extracted from the intercept to be 31 Ω.mm and 142 Ω.mm respectively. This is very large as compared to observed values for 2DEGs on AlGaN/GaN, say, which are typically <0.5 Ω.mm. These two factors – the variation in measured resistance w.r.t spacing and the high value of R_C – are indicative of the challenges involved in making low-resistance ohmic contacts to $SrTiO_3$ based 2DEGs and highlights that further research is required in order to develop low-resistance contact processes to the $SrTiO_3$ material system. In addition, the sheet resistance of the 2DEG as extracted from Hall measurements was 31.56 kΩ/sq as mentioned in the manuscript (see page 4). This enables the access resistances to be estimated as $R_{access}=R_{S,acc}+R_{D,acc} = R_{sh}*(L_{SG}+L_{GD})$ in Ω.mm. For the devices in this study, the L_{SG} and L_{DG} values were ~1.3 μm and 3.9 μm respectively, as shown in Figure 1(e) and hence R_{access}=164.112 Ω.mm.

Effect of the constriction structure and resistance quantification – In case of the constriction structure, we have wide contact pads and access resistance areas (100 μm or 0.1 mm wide) while the channel is narrow (2 and 5 μm in the present study). This affects the fractional contribution of the contact and access resistances to the channel resistance, i.e,

$$R_{tot}\ (\Omega) = 2R_C(\Omega.mm)/W_{pads}+R_{access}(\Omega.mm)/\ W_{pads}+R_{ch}(\Omega/sq)*L_{ch}/W_{ch} \qquad (S1)$$

Since the contact and access resistance widths are ~50x or 20x higher than the constriction (W_{pads}=100 μm while W_{ch} = 2 or 5 μm), the fractional contribution of the parasitic series resistance is much reduced.

For the transistor dimensions shown in Figure 1, the fractional parasitic series resistance contribution as compared to the total resistance for a planar device with width of 100 μm would be, $(2R_C/W+R_{access}/W)/(2R_C/W+ R_{access}/W+R_{ch}*L_{ch}/W)$ which even using an R_c of 30 Ω.mm and other numbers listed above works out to 74.7% (Eq. (S1) with $W_{ch}=W_{pads}$=100 μm).

For a constriction structure with 100 μm wide pads and constriction width of 2 μm, the same fractional contribution can be estimated from Eq(S1) to be 5.6%. This huge disparity is what causes the improved performance of the constriction devices as compared to the planar device.

Temperature-dependence of R_{sh} for the constriction structure –

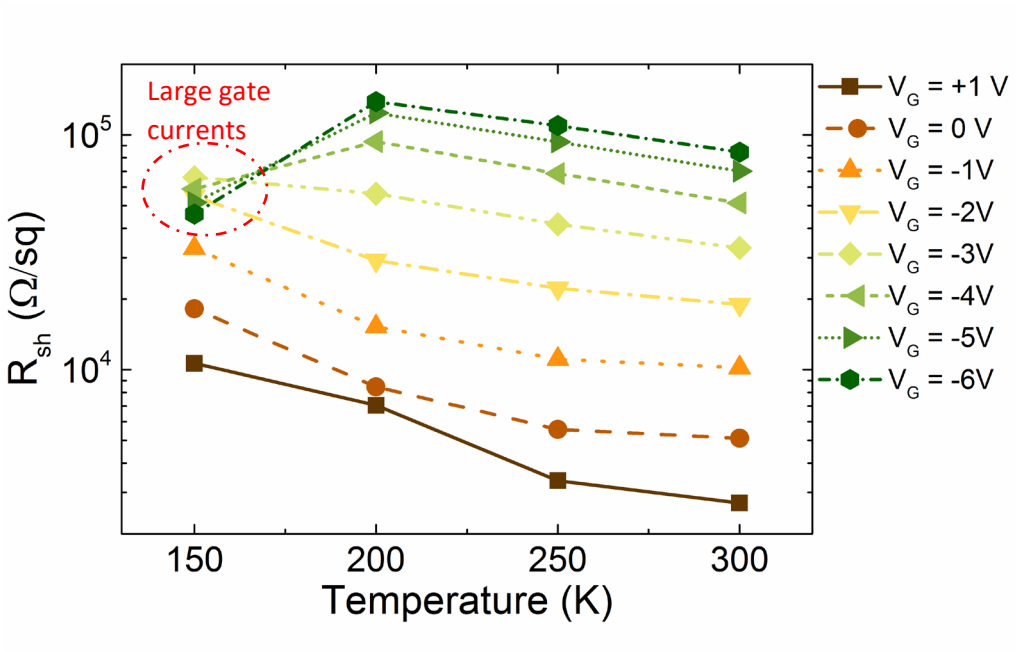

Figure S6*: Sheet resistances (in log-scale) vs temperature (linear scale) extracted from the linear region of the output curves of the 2 µm constriction transistor for gate voltages from +1V to -6V (see Figure 4 of main text) indicating the exponential dependence of R_{sh} on temperature observed for hopping transport. The decrease in R_{sh} at 150K for V_G<-3V is an artifact caused by the large gate currents.*

REFERENCES:

[1] "**Band alignments between SmTiO3, GdTiO3, and SrTiO3"** Lars Bjaalie, Angelica Azcatl, Stephen McDonnell, Christopher R. Freeze, Susanne Stemmer, Robert M.Wallace, and Chris G. Van de Walle, Journal of Vacuum Science & Technology A **34**, 061102 (2016); doi: 10.1116/1.4963833.