Supplementary information for

Unpredicted Internal Geometric Reconfiguration of An Enclosed Space Formed by Hetero-epitaxy

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This PDF file includes:
Materials and Methods
Figs. S1 to S17
References

Materials and Methods

Wafer cleaning and thermal oxide growth

6 inch (150mm) Si (001) wafers were used in our experimental work. The Si wafers are gone through a standard Radio Corporation of America (RCA) cleaning prior to thermal oxide (SiO_2) growth:

1. Organic/particle clean: $NH_4OH:H_2O_2:H_2O$ (1:1:5) at 80 ^oC for 10 minutes
2. Chemical oxide strip: $HF:H_2O$ (1:50) for 60 seconds
3. Ionic clean: $HCl:H_2O_2:H_2O$ (1:1:6) at 80 ^oC for 10 minutes
4. Chemical oxide strip and passivation: $HF:H_2O$ (1:50) for 60 seconds

Cleaned Si wafers are transferred into a tube to grow thermal oxide (SiO_2) for ~100 nm at 1000 ^oC to ensure the high quality. After SiO_2 growth, photoresist (SPR700) is coated and lithography is conducted to define the designed patterns by *i*-line lithography (exposure in wafer stepper Nikon NSR2005i9C). Once the developing is done, the exposed SiO_2 is etching down to Si by buffered oxide etch (BOE) wet etching to define the SiO_2 coated Si (100) surface for Ge epitaxy. Due to the isotropic etching, a sidewall angle of φ ~60^o is obtained (Fig. S10) where the Ge/SiO_2 interface is defined by the growth of Ge {111} facets.[1,2] Prior to germanium epi-growth, the patterned wafers are gone through the standard RCA cleaning again to ensure a clean and hydrogen-terminated surface. The final SiO_2 thickness was approximately 40 nm. Varied thickness of the oxide strips yield same lateral overgrowth, but take longer time to get coalescence for thicker oxide due to the time taken to fill the trench. The width of oxide strips is kept from 350nm to 750 nm, respectively, and the length of the oxide is from 2 μm up to 2 cm. All oxide strips are along Si <110>.

Ge growth

The wafers are introduced to an ultra-high vacuum chemical vapor deposition (UHV-CVD) batch, epitaxial growth process chamber (Leybold Sirius CVD-300). The temperature inside the hot-walled quartz tube process chamber is controlled by three separate heater zones, calibrated to maintain a flat thermal profile across the substrate boat. The base pressure in the growth chamber is around 8×10^{-9} mbar with an idle temperature of 650 ^oC. With a base pressure of that magnitude, film contamination only results from the impurity of the precursor gases. After wafer loading, temperature ramping to 800 ^oC is conducted in the chamber to get rid of any remaining native oxide and other impurities. To avoid Stranski-Krastanov roughened growth,[3] a "two-step growth" approach is employed. The low temperature Ge buffer is first grown at 350°C. Although highly defective, the buffer plastically relaxes the majority of the strain due to lattice mismatch between the Ge film and the Si substrate.[1] After growing a buffer layer thickness of 60 nm, the chamber temperature is raised to 730°C to grow Ge of higher material quality homo-epitaxially on the relaxed Ge buffer. High temperature growth is conducted using undiluted GeH_4 at a pressure of 2.0×10^{-2} mbar. At this partial pressure, Ge deposition remains selective; no nucleation is observed on the oxide mask. Thickness of the Ge epi-layers can be obtained by varying the growth time. Once the growth process finished, the process chamber is then raised to 800 ^oC to anneal the

material for 1 hour to reduce the threading dislocation density. Temperature at the process chamber is reduced to 650 ^{o}C and then the carrying boat is unloaded. To evaluate the Ge overgrowth and coalescence at different stages before coalescence, annealing at 800 ^{o}C is not conducted. All the thermal exposure is specified in the paper.

Analytical methods

Top view and cross-sections of Ge growth were observed using a high resolution scanning electron microscope (Zeiss Supra-40). Dislocations, facet orientations and tunnel profiles were carefully inspected by transmission electron microscope (TEM, JEOL-2010F), operated at 200 kV. Plan-view TEM was conducted by JEOL-2011 with a working voltage of 200 kV. The samples for TEM investigations were milled and polished to be 50- to 100-nm-thick by a focused ion beam (FIB, *FEI Helios 600*) technique (Fig. S17). Carbon was deposited to prevent the specimens from damaging by electron and ion beam. Dust may deposit on the inner walls of cavities and tunnels during the milling process. FIB was also used to thin the sample gradually to obtain the comprehensive profile information of the geometric configurations.

Supplementary Figures

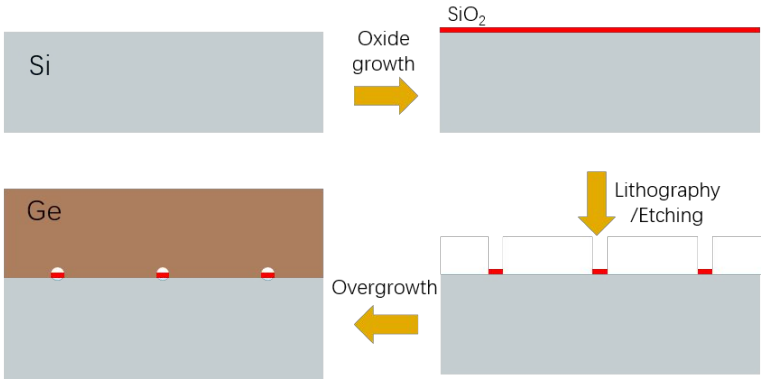

Fig. S1. Schematic process flow to form geometric configurations in the hetero-epi layer. We start from Si (100) and grow thermal oxide (SiO_2) for ~ 50 nm. Lithography technique was used to define the dimension of the oxide strips with width from 350 nm to 750 nm and length from 2 μm to 20 μm, are aligned along the Si <110> directions. Ge growth is then conducted in an UHVCVD system.

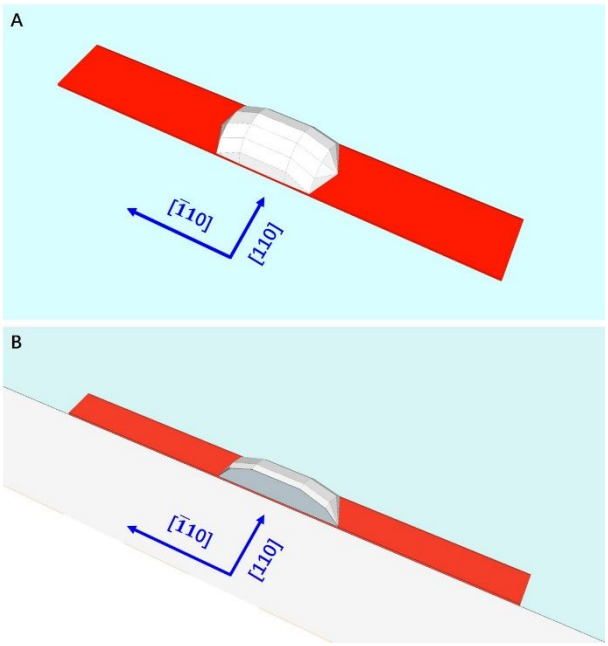

Fig. S2. (**A**) Schematic view of geometric configurations formed above oxide stripe during Ge epitaxy growth on Si (100). The FIB milling is conducted along both Si[110] and Si [$\bar{1}$10] directions to visualize the whole structure. (**B**) Cut in the center along Si[110] direction of the geometric configurations.

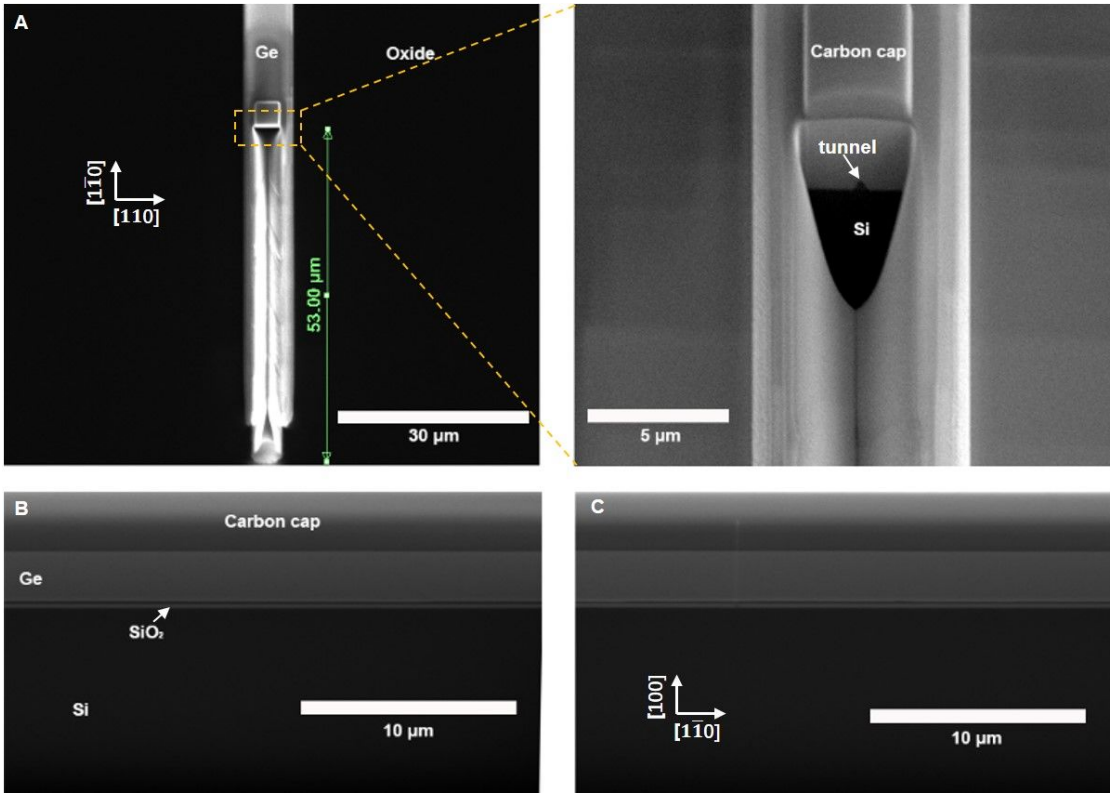

Fig. S3. "Infinite" long tunnel on oxide strip. We have selectively grown Ge on oxide patterned Si (100) wafer. The oxide strip is designed to be 2-cm long. (**A**) Top view of the Ge selectively grown on oxide patterned Si (100) surface at one end of the oxide strip. We have used FIG to milling along the Ge along Si [$\bar{1}$10] direction up to 53 µm and always observe the tunnel structure. The tunnel can be seen in the enlarge view in the Fig. 1(A) which was taken at an inclination of 52°. Carbon is deposited on the Ge to protect the Ge surface for ion milling. We have randomly chosen several locations to check if tunnel is formed between Ge and oxide strip. It has been found a tunnel structure is formed at every checking location. (**B** and **C**) show two random locations where the tunnel can be observed from the cross-section SEM view.

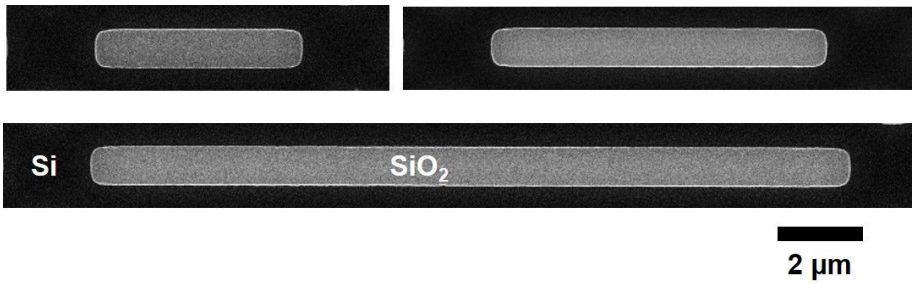

Fig. S4. Oxide strips patterned on Si (100) along Si [$\bar{1}$10]. The length of the oxide strip is around 4, 8 and 18 µm.

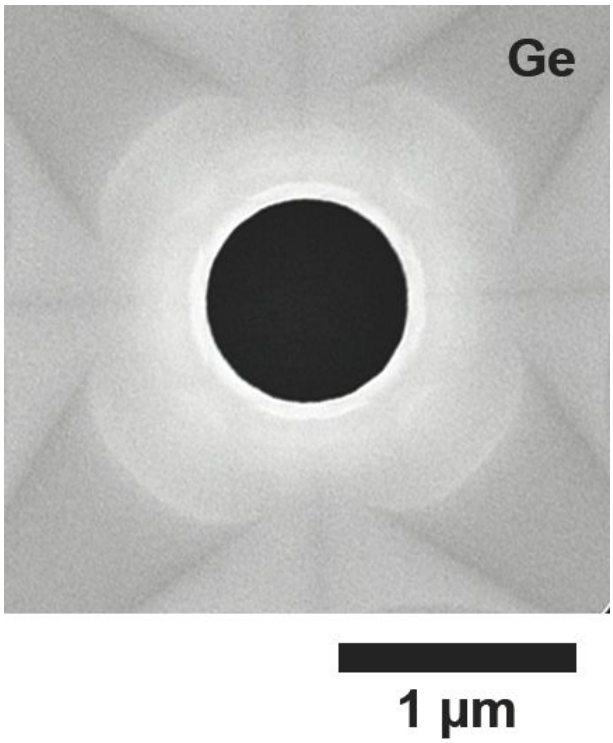

Fig. S5. Ge overgrown on SiO_2 strip. The black part is oxide strip underneath. It can be seen that the final Ge coalescence is progressing isotropically

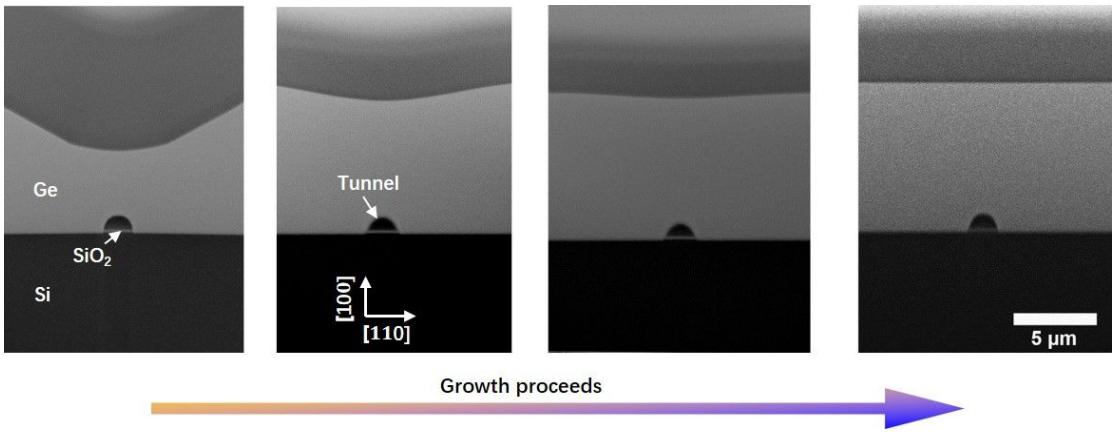

Fig. S6. SEM cross-section view of Ge lateral overgrowth on oxide strips in a sequence of progressing growth stages after the oxide strip is sealed.

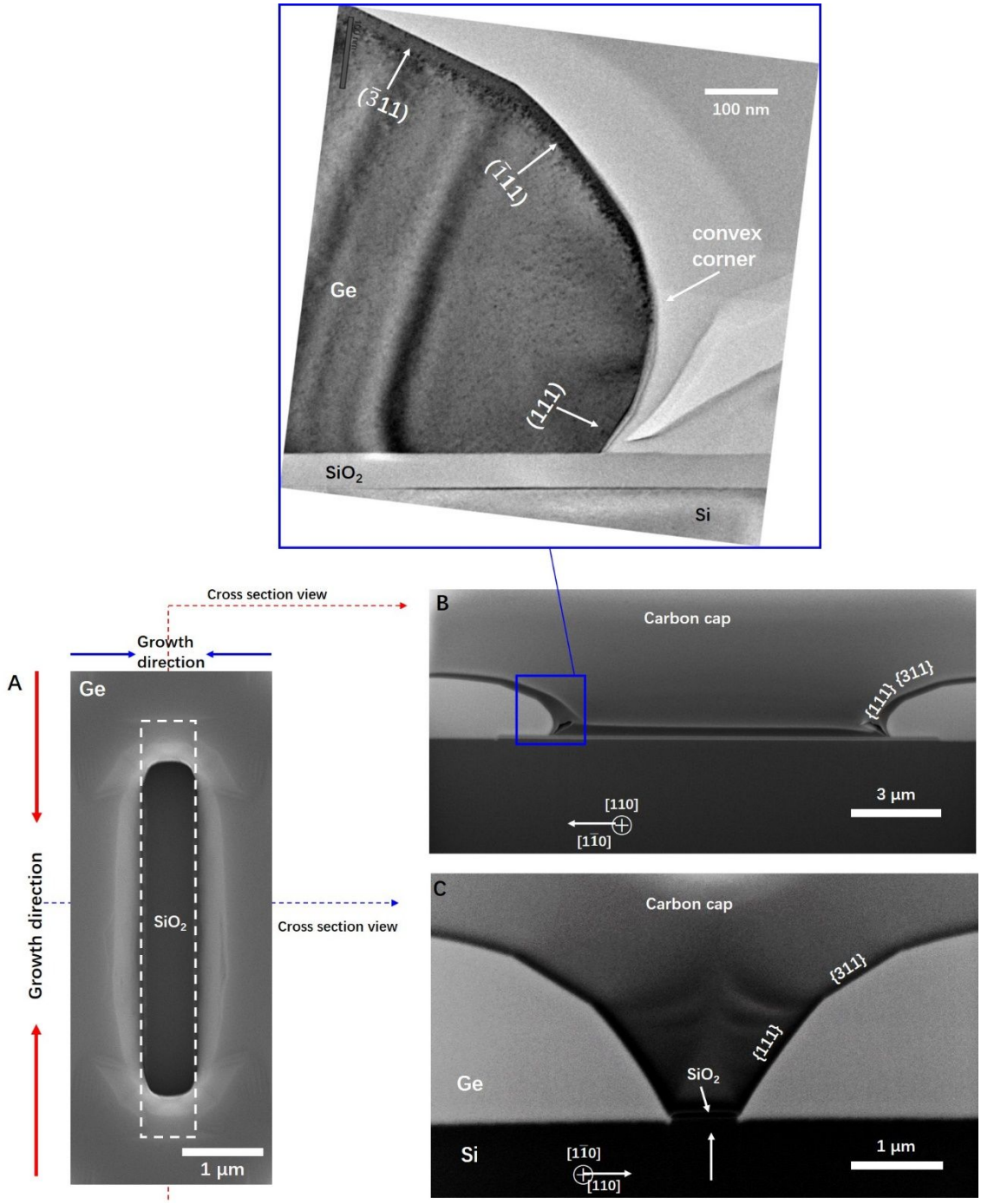

Fig. S7. Ge lateral overgrowth. The oxide stripe is 8 μm in length and 750 nm in width. Lateral overgrowth in both Si [110] and [$\bar{1}$10] directions, as shown in (**A**). (**B**) Cross-section view in Si [110] direction by cutting in center, showing two growth fronts are approaching in opposite directions. An enlarged view demonstrates the growth front in confined by (311), (111) and ($\bar{1}$ 11) facets, where joint of (111) and ($\bar{1}$11) facets are separated by a convex corner. (**C**) Cross-section view in Si [$\bar{1}$10] direction, showing the {111} and {311} facets defined growth fronts.

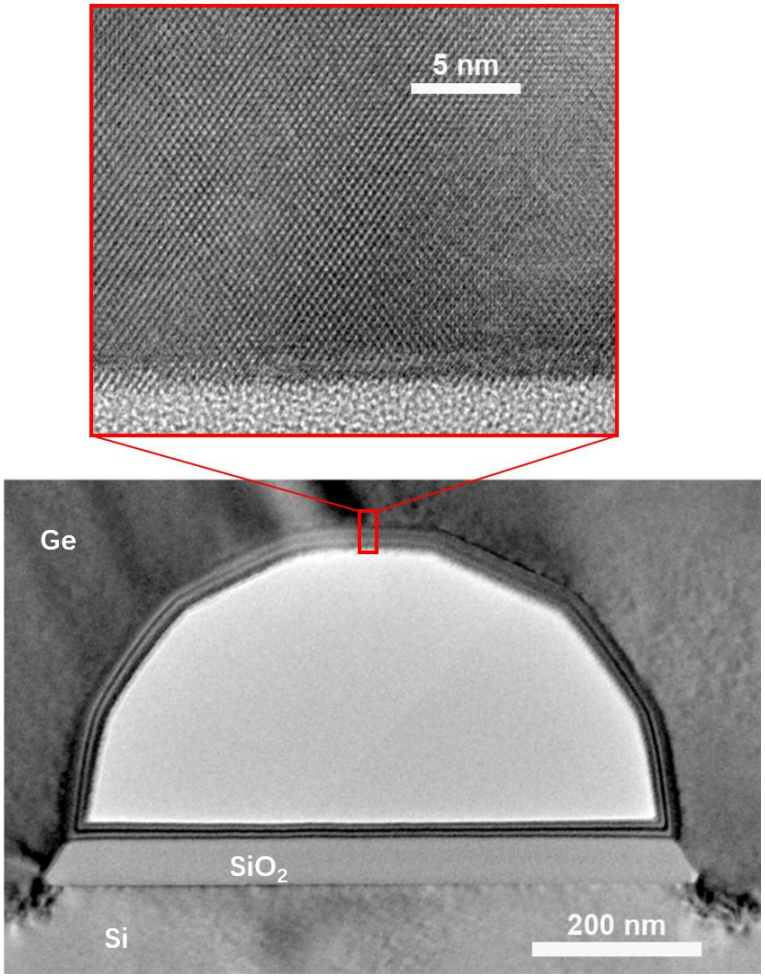

Fig. S8. HR-TEM image of the Ge, enlarged from **Fig. 2E**, demonstrating a perfect crystalline upon coalescence. The inner wall of the tunnel is near atomically flat.

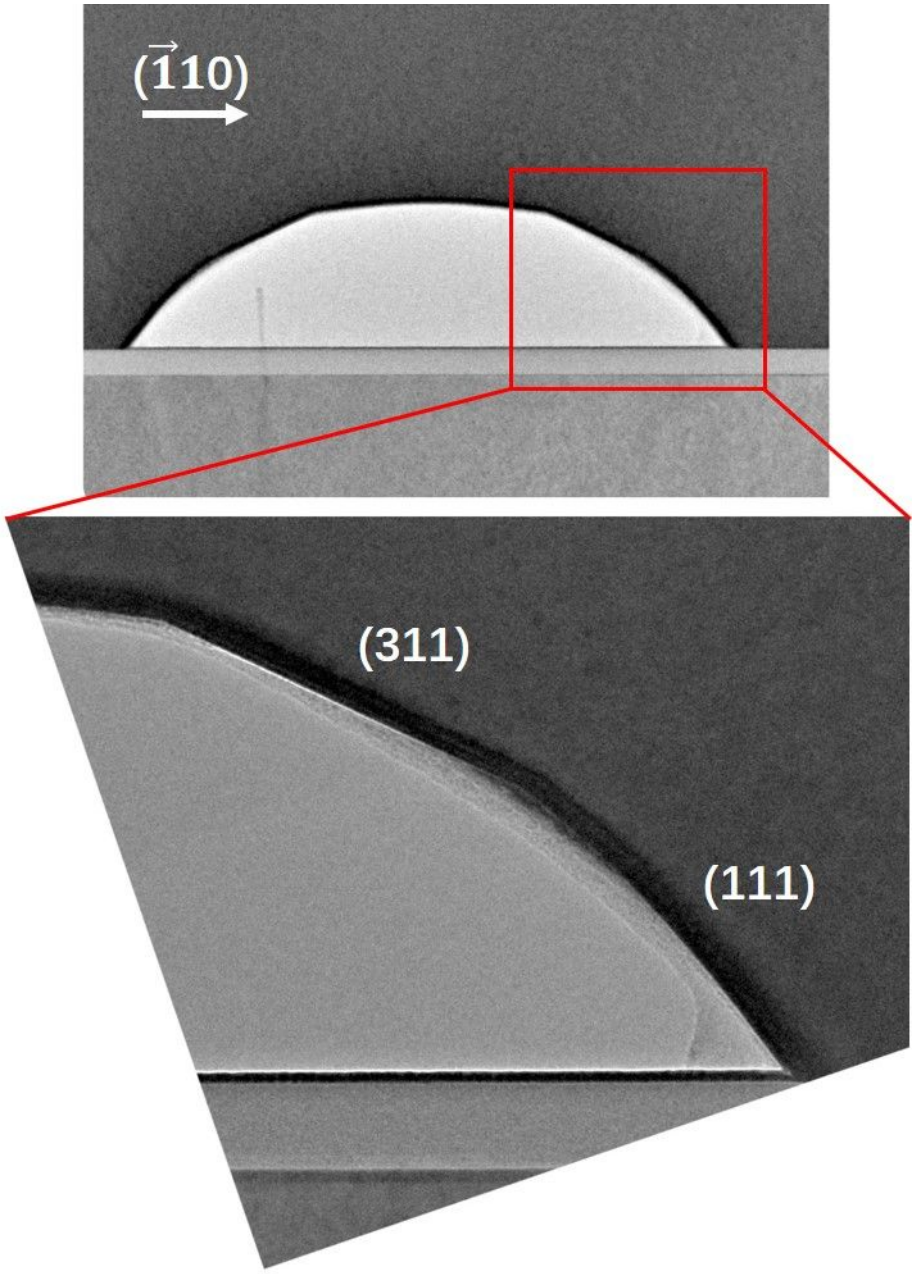

Fig. S9. TEM view in the center of a cavity along Si [$\bar{1}$10]. The length of the oxide strip is 6-μm-long. The cavity end is defined by {311} and {111} facets.

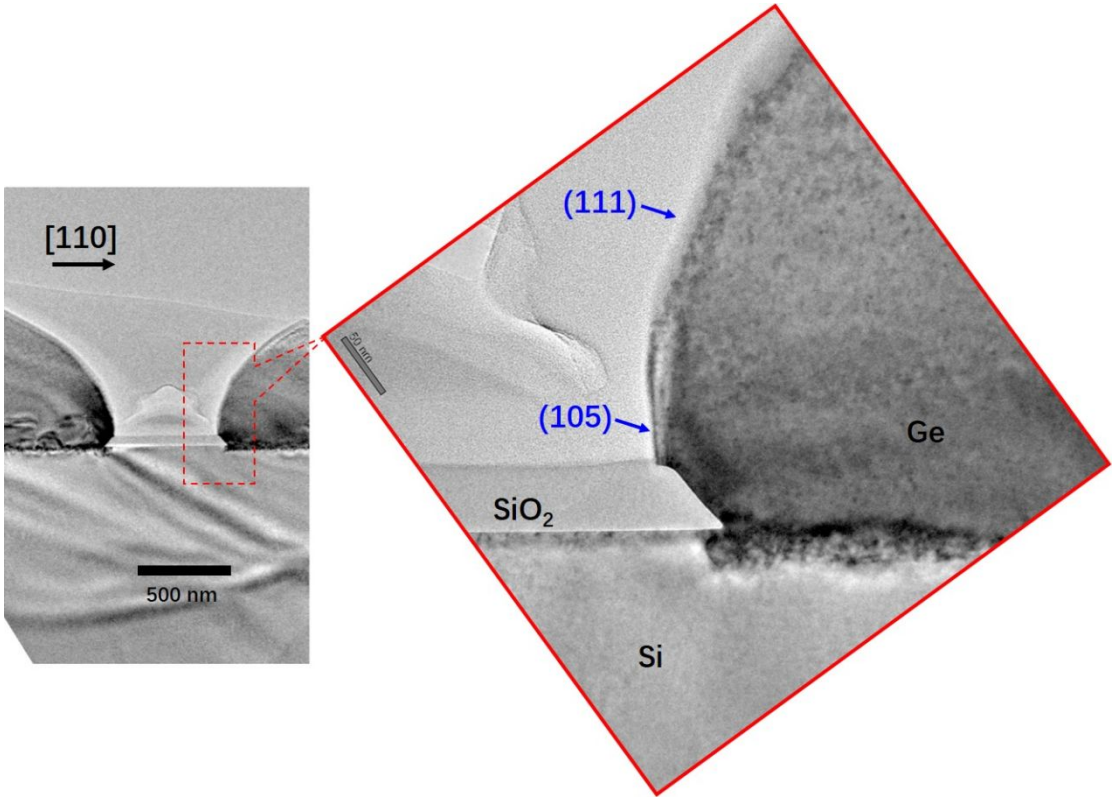

Fig. S10. Cross-section view in Si [110] direction before Ge coalescence. Ge lateral overgrowth along Si [110] is observed. Ge (105) facet appears to shrink the length of (111) facet in order to avoid the direct Ge/SiO_2 contact

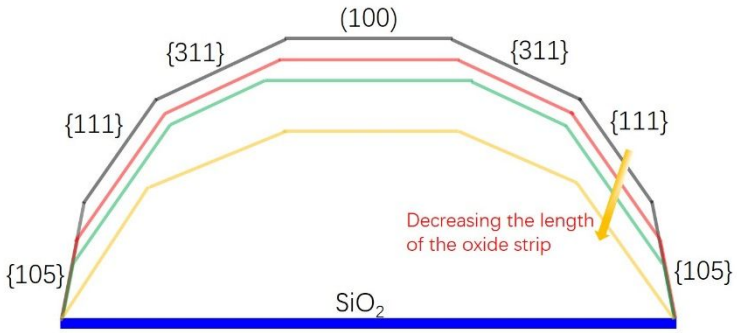

Fig. S11. Schematic model of a cavity center when viewing along the Si [$\bar{1}$10] direction. The height of {105} facets decreases as the length of the oxide shorting.

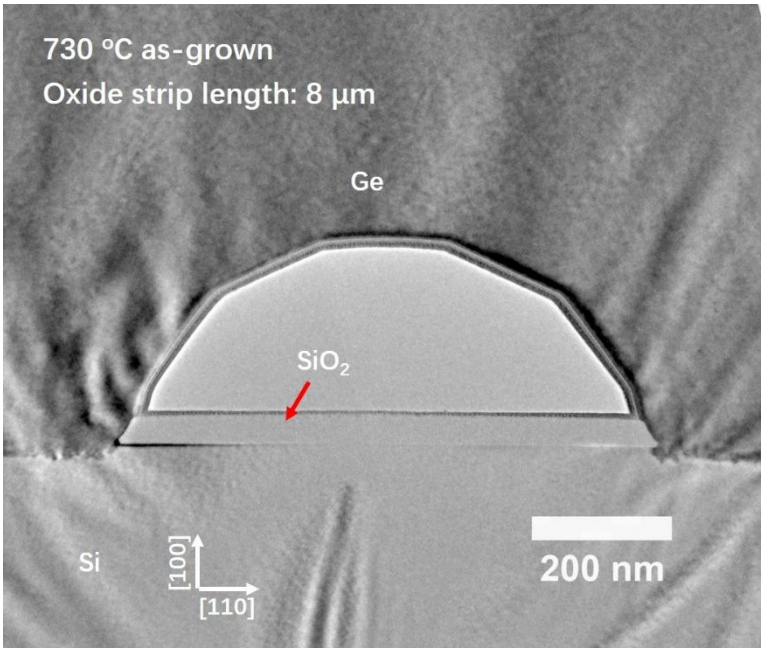

Fig. S12. Cross-section TEM view in the center of a cavity along Si [$\bar{1}$10] after epi-growth at 730 °C. The length of the oxide strip is 8-µm-long.

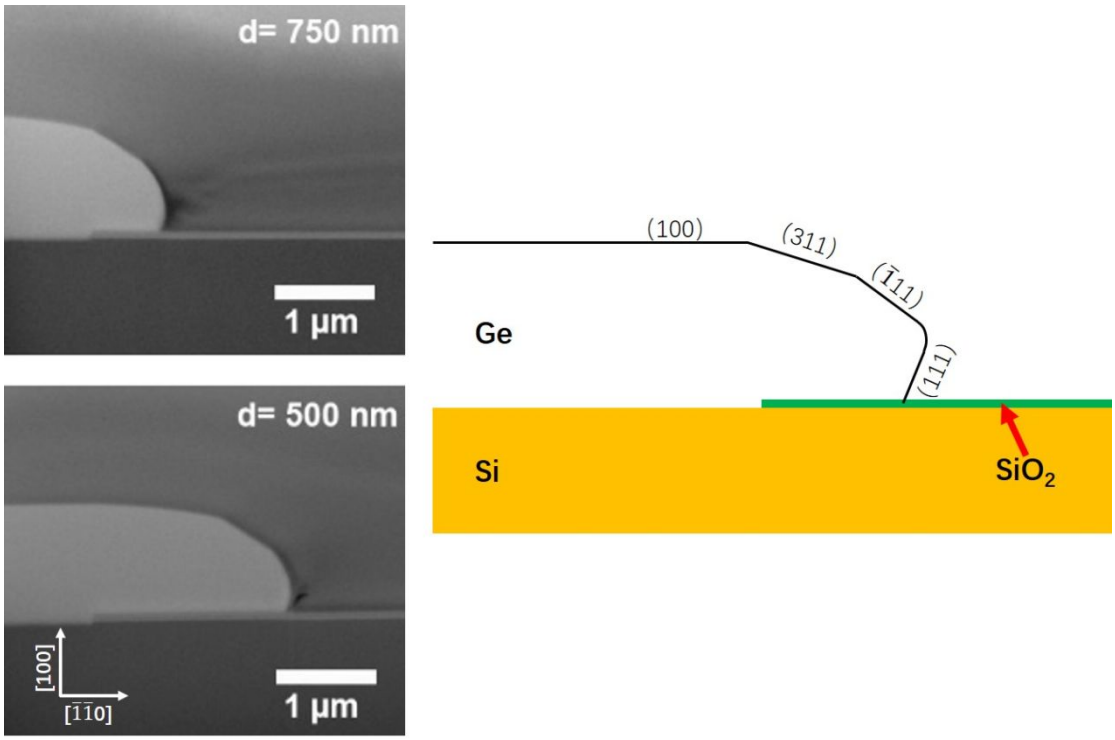

Fig. S13. Accelerated overgrowth along Si [$\bar{1}$10] with oxide stripes of 750 nm and 500 nm, respectively. Give identical growth time, Ge later overgrowth above oxide strips with width of 500 nm is much faster than the one with width of 750 nm.

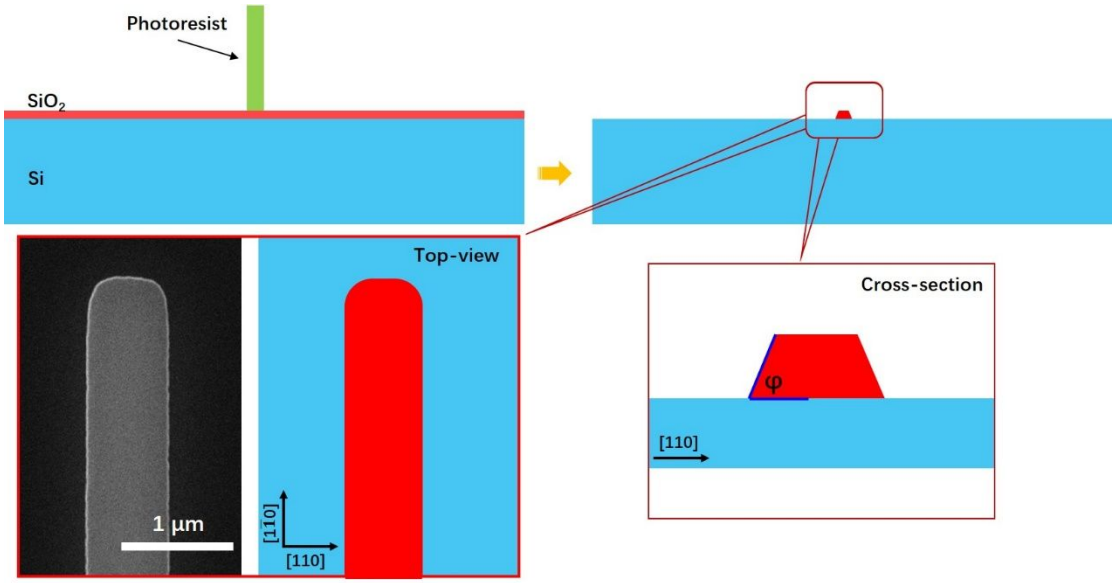

Fig. S14. Defining the oxide stripes on Si (100). After thermal oxide grown on Si (100), photoresist coated on the wafer and lithography is used to define the oxide stripes. Because of resolution limitations of *i*-stepper lithography, unavoidable rounded corners with concave and zero curvature sections in the end of oxide mask create complex facetted regions. In order to get a clean Si surface, HF is used in the last step to wet etch away the SiO_2. Due to the isotropic etching, a sidewall angle of φ of ~60 ^{o} is obtained. It has been reported when the sidewall angle φ<82.5^{o}, Ge/SiO_2 interface is defined by the growth of {111} facets; once φ>82.5^{o}, the interface is governed by {311} facets.(*1*)

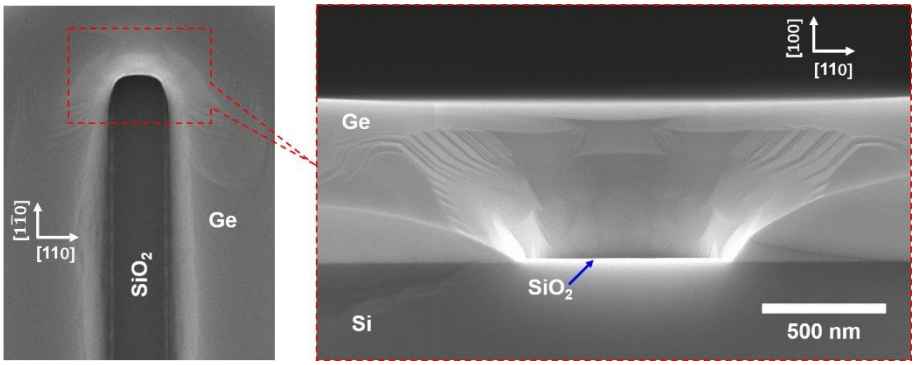

Fig. S15. Ge overgrows in Si [$\bar{1}$10] direction. As indicated by the red dash square, enlarged SEM image from cross-section view clearly shows there are multiple growing facets defines the growth front in Si [$\bar{1}$10] direction.

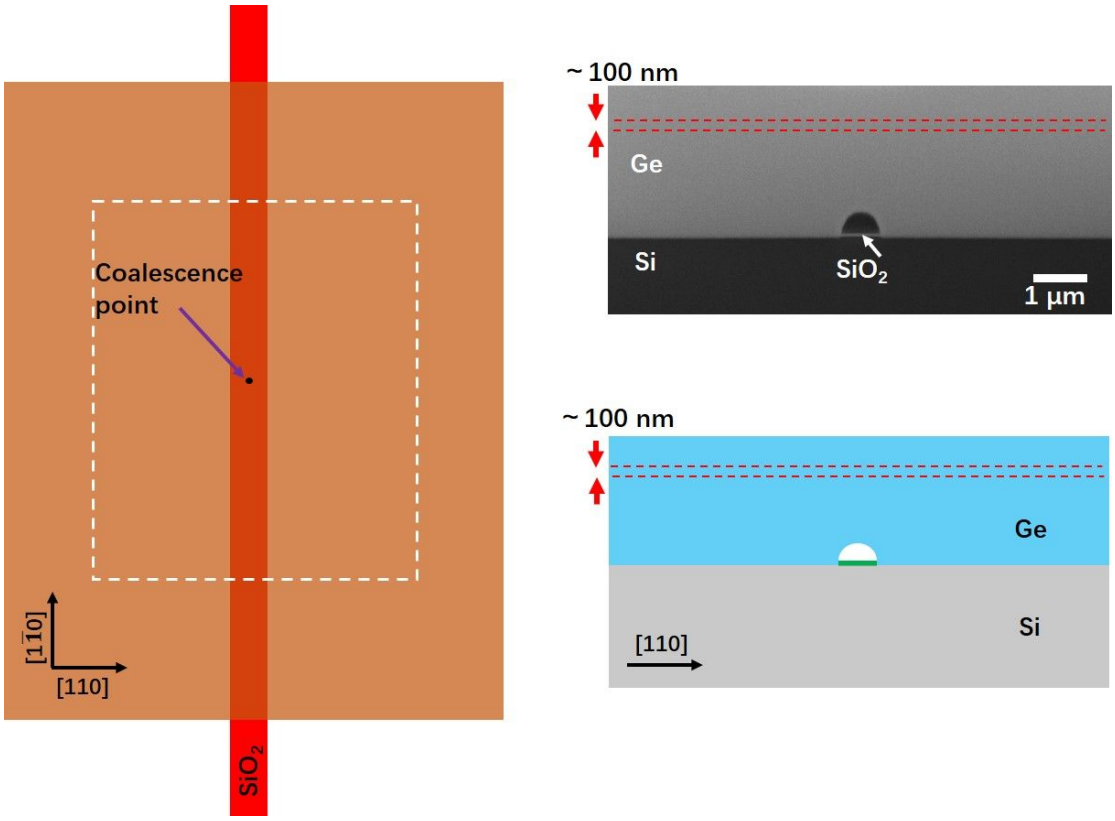

Fig. S16. Plan-view TEM sample preparation. 8x5 μm^2 Ge layer is cut for preparing the plan-view TEM. The Ge layer in the vertical direction is shown, which is above the cavity or tunnel. The thickness of the Ge layer after ion milling is about 100 nm. From the top view, both samples include the coalescence point and coalescence line which are kept in the center part of the samples.

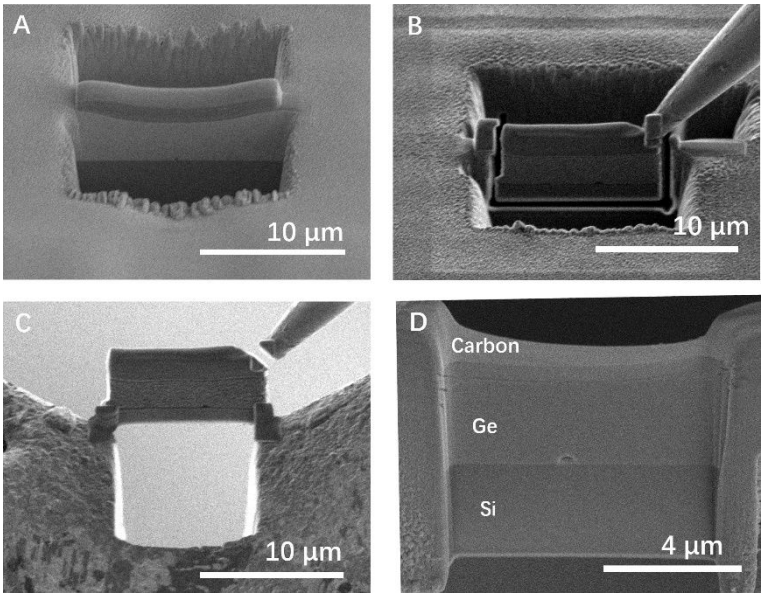

Fig. S17. Cross section TEM sample preparation. SEM images were recorded during the FIB milling, sample transfer and polishing. Since the SiO_2 location is marked, it is easy to find and select the area for TEM sample preparation. A protective carbon cap is deposited *in situ* (**A**) and the surrounding region is then milled out through Ga^+ ion beam. Once the milling is finished, tungsten probe is employed to transfer the sample to copper grid. The tungsten probe is welded to the sample before cutting the last connection (**B**). The sample is transferred to a copper grid through welding to the post with carbon. Once the sample is confirmed to be well bonded to the copper grid, the tungsten probe is then cut for separation (**C**). The sample is eventually thinned to be 50-100 nm though the Ga^+ ion beam.

References

1. J. Liu, GeSi Photodetectors and Electro-absorption Modulators for Si Electronic-photonic Integrated Circuits. *Massachusetts Inst. Technol.* (**2007**).
2. Bai,J.; Park, J.-S.; Cheng, Z.; Curtin, M.; Adekore, B.; Carroll, M.; Lochtefeld, A. *Appl. Phys. Lett.* **2007**, 90, 101902.
3. Wulff, G.. *Zeitschrift für Kryst. und Mineral.* **1901**, 34, 449–530.