Supporting Information

Molecularly thin electrolyte for all-solid-state non-volatile two-dimensional crystal memory

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Part 1. CoCrPc monolayer deposition on MoS_2 and WSe_2

AFM images of MoS_2 and WSe_2 flakes partially covered in the CoCrPc monolayer are shown in **Figure S1** (a) and (b), respectively. The partial coverage is purposeful because it allows us to measure the thickness of a single CoCrPc layer. The deposition was achieved by drop-casting 44 µL of a 13 mg/L CoCrPc solution (CoCrPc dissolved in benzene/ethanol, 9:1 v/v) on a 1 × 1 cm^2 Si chip (90 nm SiO_2) covered in exfoliated flakes of either MoS_2 or WSe_2. This is followed by a 30-min anneal in Argon at 220 °C. As shown in the line scans below, the thickness of CoCrPc is confirmed as ~ 0.5 nm, which is in good agreement with the expected thickness based on DFT calculations and previously published monolayer thicknesses on HOPG.[1]

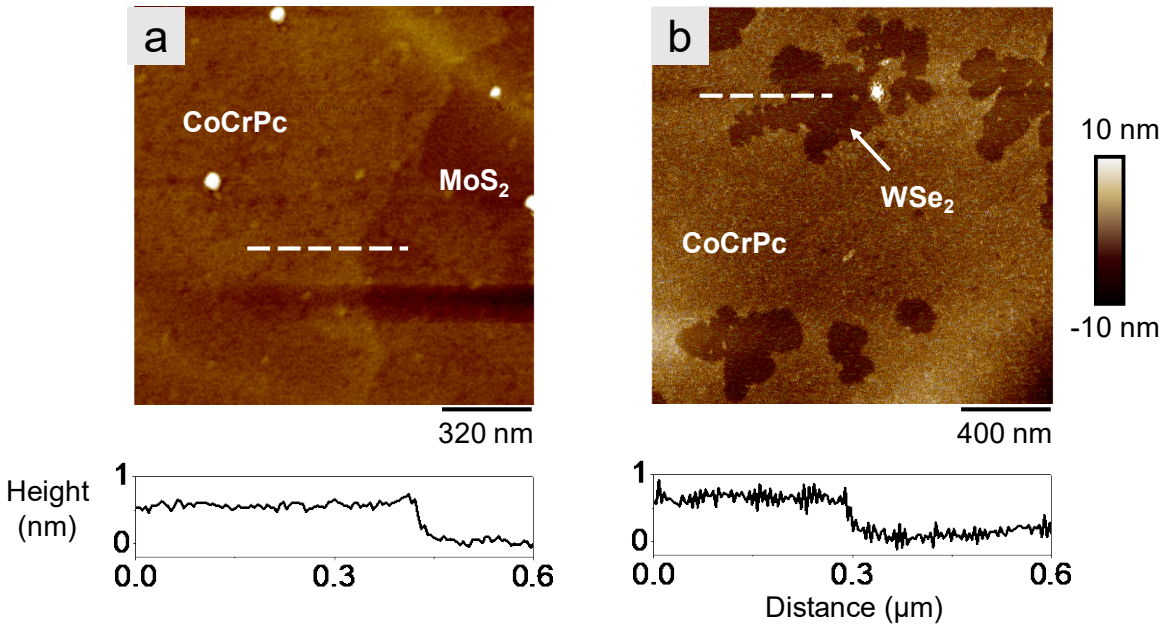

Figure S1. Monolayer CoCrPc on MoS_2 and WSe_2. AFM topology (height) of exfoliated **(a)** MoS_2 and **(b)** WSe_2 flakes with partial coverage of CoCrPc to measure the thickness of CoCrPc. For each substrate material, the line scan is shown below each AFM image, with the corresponding position indicated by the white dashed line.

Part 2. Optimization of CoCrPc monolayer deposition on WSe_2

The volume of the CoCrPc solution deposited per unit area (i.e. the dose) and the annealing temperature must be optimized to deposit a uniform, single molecular layer of CoCrPc on a 2D surface.[1] As mentioned above, a CoCrPc solution of 13 mg per liter of benzene/ethanol (9:1 v/v) is used. As shown below, the CoCrPc dose and annealing temperature are optimized for monolayer deposition on WSe_2.

Figure S2 (b) – (d) show the impact of CoCrPc dose on the coverage, where the dose of CoCrPc increases from 38 to 52 μL/cm^2. CoCrPc molecules form a discontinuous monolayer with ~ 0.5 nm thickness when the concentration is too low (e.g., 38 μL/cm^2 in (b)). In contrast, when the concentration is too high (e.g., 52 μL/cm^2) full coverage of the first layer is achieved, but a second layer forms on top of the first layer as shown in (d). The concentration that gives full coverage of a single monolayer is optimized as 50 μL/cm^2.

In the annealing temperature range of 220 – 260 °C, aggregates of CoCrPc are minimized at 240 °C, as shown in Figure S2 (a), (c) and (e). Thus, the optimal deposition conditions for the monolayer with full coverage on WSe_2 is achieved with the dose of 50 μL/cm^2 and annealing temperature of 240 °C.

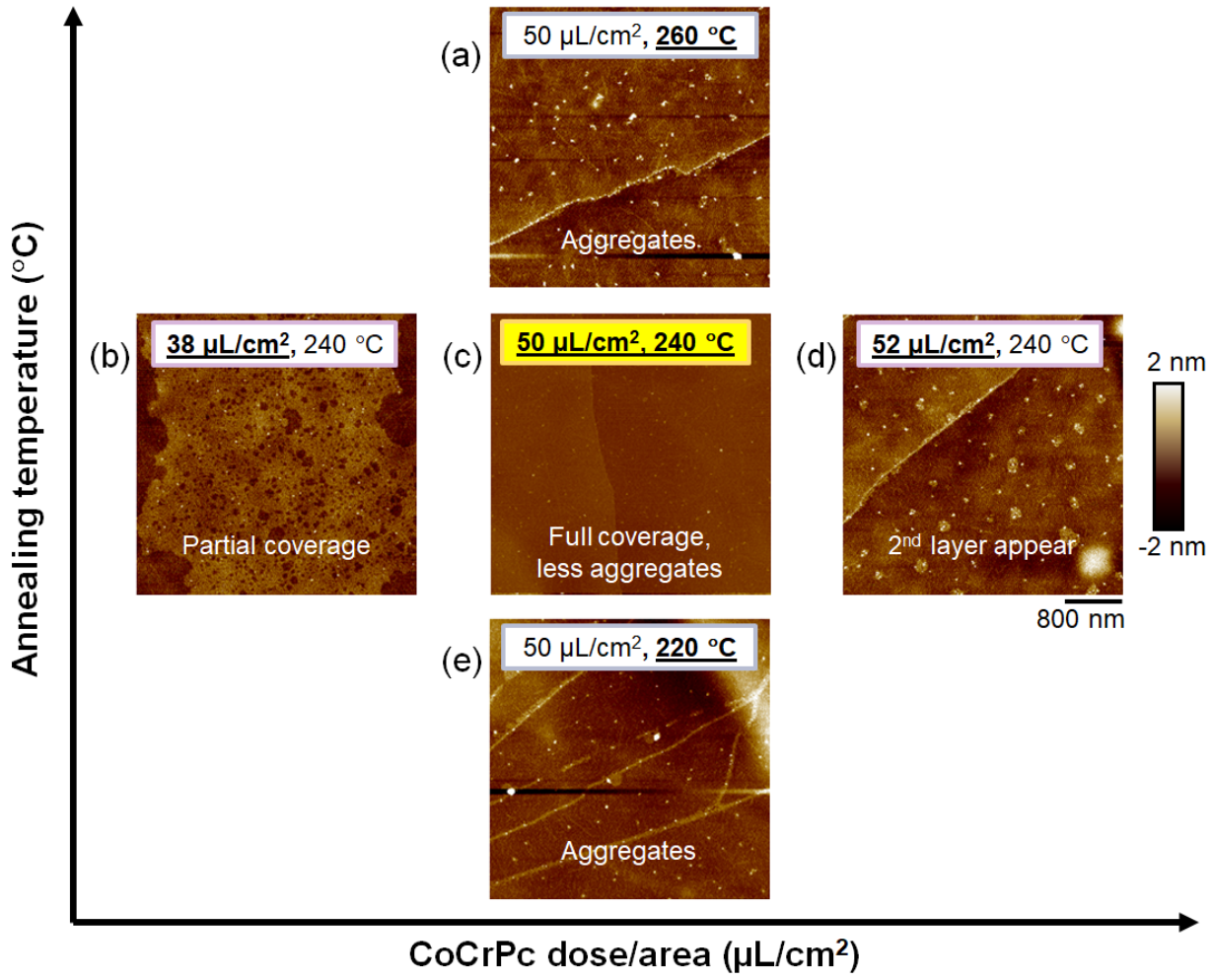

Figure S2. Optimization of the deposition conditions for a monolayer CoCrPc on WSe_2. AFM topology scans of the CoCrPc monolayer on WSe_2 flakes prepared by drop casting 13 mg/L CoCrPc benzene-ethanol solution (9:1 v/v) on 1×1 cm^2 chip, and by annealing for 30 min in Argon. Left to right: increasing the volume of CoCrPc solution drop-casted on the 1 cm^2 chip to increase the coverage of CoCrPc from **(b)** partial coverage to **(d)** full coverage with the 2nd layer of CoCrPc starting to form. Top to bottom: optimizing the annealing temperature to minimize the amount of CoCrPc aggregates (white particles in **(a)** and **(e)**). The optimized deposition condition is shown in **(c)**. Note that the step edges in (b) – (e) correspond to the WSe_2 layers (not CoCrPc).

Part 3. DFT calculations

The stability of the *off*-state with and without h-BN was estimated by the first principles calculations based on density functional theory using the Vienna *ab initio* simulation package (VASP).[2,3] The local density approximation (LDA) was carried out to describe the exchange-correlation potentials.[4] An energy cutoff of 500 eV was used. The different configurations were fully optimized with a Monkhorst-Pack *k*-point mesh of 3 × 3 × 1. The converged criterion in structural relaxation was the remnant force on each atom less than 0.02 eV/Å.

To obtain the energetically favorable structure, the adsorption energy (E_{ad}) is calculated according to the formula $E_{ad} = E_{total} - E_{WSe2} - E_{h\text{-}BN} - E_{adsorbate}$, where E_{total}, E_{WSe2}, $E_{h\text{-}BN}$, $E_{adsorbate}$ are the total energies for the whole system, the pristine WSe_2, h-BN, and CE-Li^+ complex, respectively. The negative E_{ad} indicates that the WSe_2/CE-Li^+/h-BN structures are stable with a higher absolute value indicating a more favorable state.

To identify the energetically favorable locations of Li^+/CE on the WSe_2 surface, three configurations were considered: Li^+/CE located above the 1) W atom, 2) Se atom and 3) hollow site of WSe_2, denoted as T_W, T_{Se}, and C_1. Similarly, for h-BN, three configurations were considered: Li^+/CE located above the 1) B atom, 2) N atom and 3) hollow site of h-BN, denoted as T_B, T_N, and C_2. By comparing the adsorption energies in all three configurations, the T_W and center site (C_2) are found as the most stable configurations for Li^+/CE on WSe_2 and CE/Li^+ on h-BN, respectively.

For the entire WSe_2/CE-Li^+/h-BN stack, a 4 × 4 monolayer WSe_2 supercell and a $2\sqrt{7} \times 2\sqrt{7}$ h-BN supercell were used to build the supercell to match their lattice constants. The overall lattice constant of WSe_2/ CE-Li^+/h-BN was set to be 13.15 Å. The calculated E_{ad} after adding h-BN is -

5.15 eV, representing an increase in the absolute value of 1.34 eV compared to that without h-BN (-3.81 eV). This result indicates the stability of the *off*-state is improved in the WSe_2/CE-Li^+/h-BN stack.

The detailed structural parameters are provided in **Table S1**, including the distance from the plane of the oxygen atoms and Li^+ in the CE to WSe_2 or h-BN (i.e., $d_{O\text{-}W/N}$ and $d_{Li^+\,W/N}$) as well as the distance between the Li^+ and O atoms (d_{O-Li^+}).

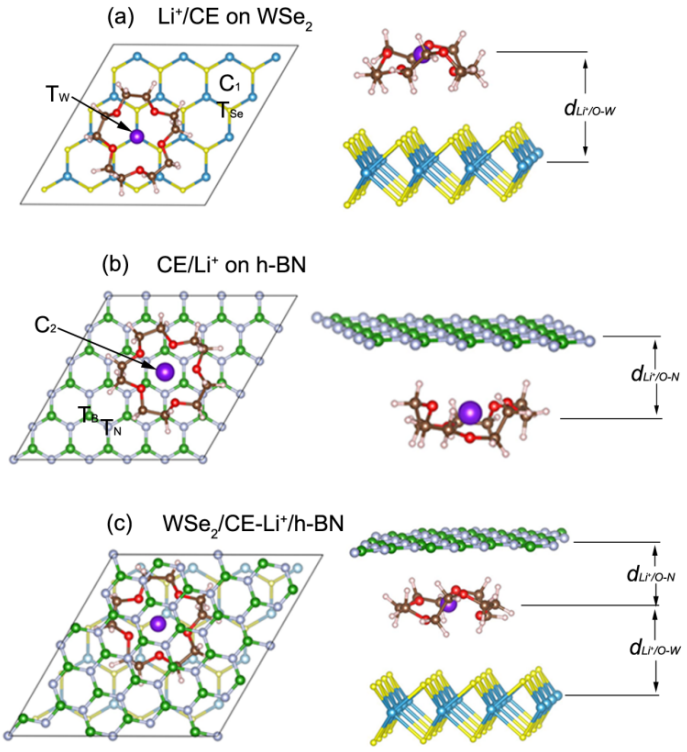

Figure S3. DFT simulation. Top and side views of different configurations for **(a)** Li^+/CE on WSe_2, **(b)** CE/Li^+ on h-BN, and **(c)** WSe_2/CE-Li^+/h-BN.

Table S1. Adsorption energy (E_{ad}) and structural parameters for Li^+/CE/WSe_2, CE/Li^+/h-BN, and WSe_2/CE-Li^+/h-BN configurations.

System	Site	E_{ad} (eV)	$d_{O\text{-}W/N}$ (Å)	$d_{Li^+\text{-}W/N}$ (Å)	d_{O-Li^+} (Å)
Li^+/CE/WSe_2	T_W	-3.81	5.77	5.99	2.17
CE/Li^+/h-BN	C_2	-2.67	3.64	3.53	2.07
WSe_2/CE-Li^+/h-BN	C_2	-5.15	6.03/3.68	6.06/3.66	2.07

DFT calculations of the energy barrier to switching with the h-BN cap in the absence of an applied field are presented in **Figure S4** where the energy is normalized to the *on*-state energy. The barrier is predicted as ~0.6 eV which corresponds to a switching speed of ~ ms according to attempt frequency analysis reported previously.[5] However, as discussed in the manuscript, the minimum retention time measured experimentally exceeds hours, meaning that the DFT calculations are underestimating the energy barrier. In addition to the barrier, the relative energies of the *on*- and *off*-state are shown in Figure S4, where the off-state is 40 meV larger than the *on*-state.

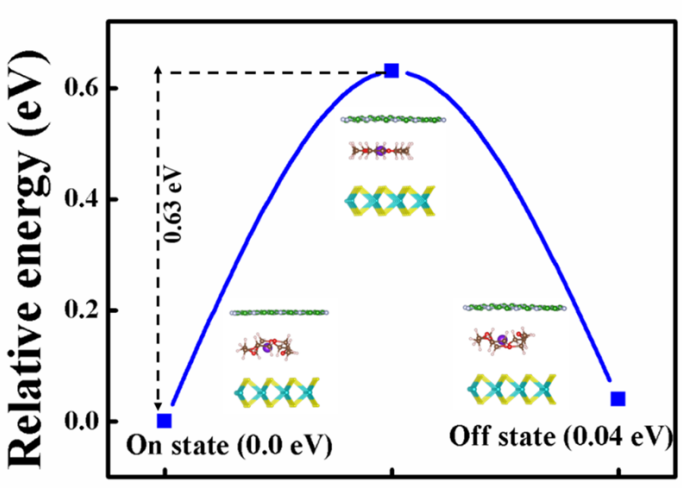

Figure S4. Relative energy of WSe_2/CE-Li^+/h-BN system corresponding to *on*- and *off*-state of MERAM. Insets are the cross-sectional views of three configurations for WSe_2/CE-Li^+/h-BN system: *on*-, transient, and *off*-state.

Part 4. Removal of e-beam resist residue on WSe_2 channel by AFM contact mode cleaning

To remove e-beam resist residue on the WSe_2 FET channel, AFM contact-mode cleaning was performed using a Bruker Dimension Icon AFM inside an MBraun glovebox.[6] The polymer residue was push away from the FET channel by the AFM tip (SCM-PIT-v2, 3 N m^{-1}) during scanning in contact mode. **Figure S5** (a) and (b) show the surface topology of a representative WSe_2 FET measured by AFM before and after the AFM cleaning, respectively, to confirm the removal of the residue. The surface roughness was averaged over 6 locations for both the channel surface before and after the cleaning (one of the six locations is indicated by the blue squares on the scan images). The roughness was reduced from 0.82 ± 0.02 to 0.23 ± 0.04 nm after the AFM cleaning, which is close to the roughness of freshly exfoliated WSe_2 (0.24 ± 0.02 nm).[6]

As shown in Figure S5 (c) and (d), current-voltage measurements of the WSe_2 FETs were made before (black lines) and after AFM cleaning (red lines) in the vacuum probe station using a Keysight B1500A semiconductor parameter analyzer. the transfer characteristics (I_D-V_{BG}) show that the AFM cleaning does not degrade the maximum current and mobility of WSe_2 FETs.

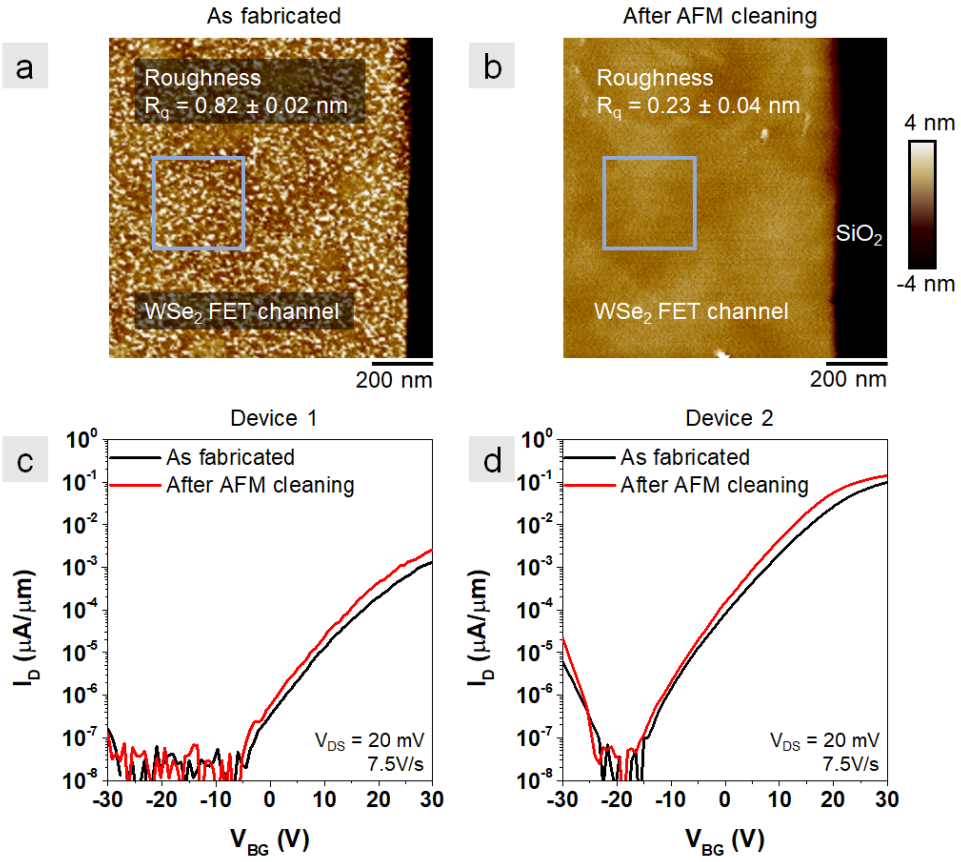

Figure S5. Removing e-beam resist residue by AFM contact-mode cleaning. AFM topology scan of one WSe_2 FET channel **(a)** as fabricated and **(b)** after AFM cleaning. The averaged roughness (R_q) values are reported where the error represents one standard deviation from the mean. The R_q values were calculated based on 6 different locations, with one of the locations indicated by the 300 × 300 nm blue box. Transfer characteristics of WSe_2 FETs as fabricated (black lines) and after AFM cleaning (red lines) are shown in **(c)** for Device 1 and **(d)** for Device 2.

Part 5. Conductive AFM of CoCrPc monolayer

To demonstrate that CoCrPc is electrically insulating, conductive AFM using the Bruker Peakforce Tuna module was performed on a graphite substrate (HOPG) with partially covered CoCrPc monolayer. The topography of a HOPG region with discontinuous CoCrPc coating is shown in **Figure S6** (a). The corresponding adhesion mapping is shown in (b), where the CoCrPc coated region (appears as darker) is less adhesive to the AFM tip than the exposed HOPG (brighter). The adhesion mapping is almost independent of changes in height and only sensitive to surface intrinsic adhesion, which helps us to distinguish the uncoated region from the HOPG step edges. In Figure S6 (c), the bare HOPG region has tunneling current (exceeding 1 pA), while the region covered with a CoCrPc monolayer has ~ 0 tunneling current. This result is sensible because CoCrPc is electrically insulating and prevents current flowing from conductive AFM tip to HOPG substrate.

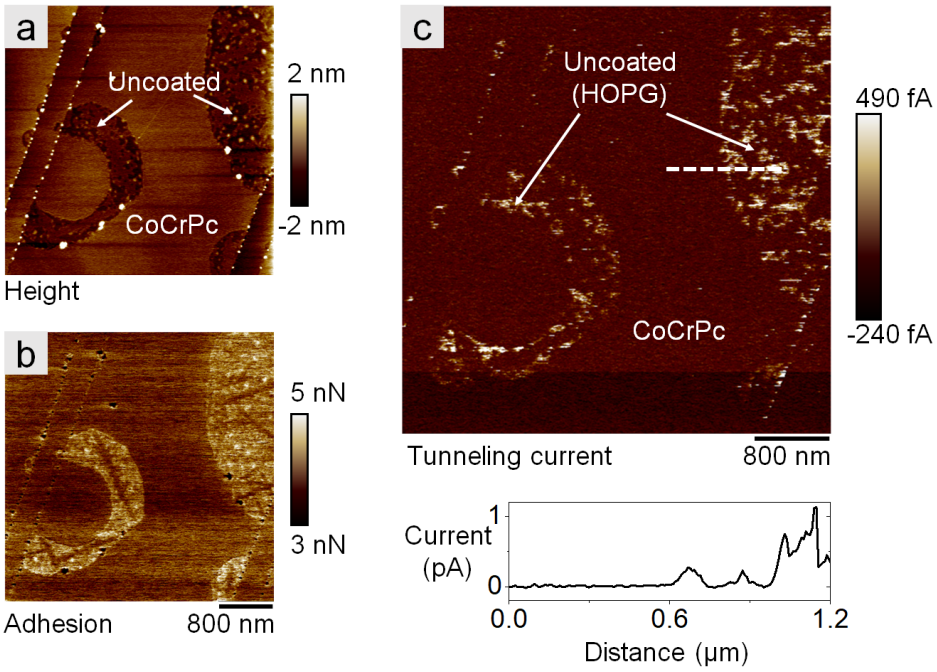

Figure S6. AFM images of topology, adhesion and conductivity for CoCrPc on graphite (HOPG). (a) AFM topology (height) of CoCrPc coated and uncoated regions on HOPG. **(b)** Adhesion of CoCrPc coated and uncoated regions on HOPG, showing that the uncoated region (i.e., bare HOPG) has a higher adhesion with the AFM tip. **(c)** Tunneling current mapping measured by conductive AFM (Peakforce Tuna), with an applied voltage of 800 mV. The line scan of the tunneling current is shown below the scan where the line scan position is indicated by a dashed line in (c).

Part 6. Transfer measurements and analysis

As shown in **Figure S7**, programming tests were conducted on the same WSe_2 FET (a) before, (b) after CoCrPc deposition (c) after $LiClO_4$ deposition and (d) after capping with few-layer h-BN. On the bare FETs, the opening between the transfer curves after programming is nearly identical to the intrinsic hysteresis measured without any programming applied. However, by adding a monolayer of CoCrPc, the magnitude of the shift between the two transfer curves after programming increases, showing that CoCrPc itself already has some degree of bistability, as reported previously on graphene.[7] The magnitude further increases by adding Li^+ the CoCrPc to achieve stronger the desired doping effect. After capping the channel with few-layer h-BN, the bistability is enhanced significantly, reflected by an additional shift of the transfer curve towards positive V_{BG} after programming *off*.

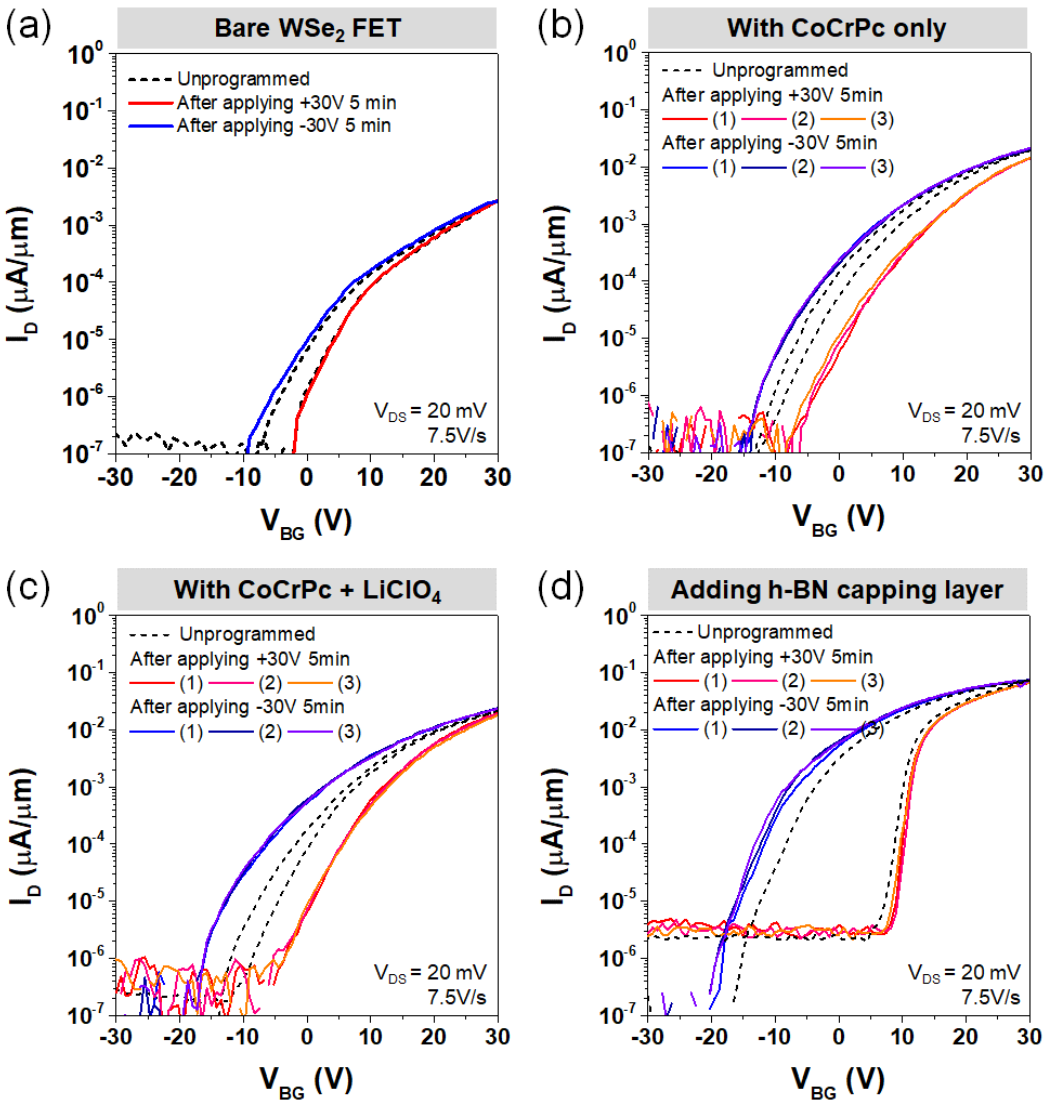

Figure S7. Transfer characteristics of a backgated WSe_2 FET with programming tests conducted under four conditions. (a) Programming tests on the WSe_2 FET after vacuum anneal without the electrolyte (i.e., bare WSe_2). The unprogrammed condition is marked as black dotted line, and the transfer curves after programming are marked as red for programming *off* and blue for programming *on*. **(b)** Programming tests after depositing only CoCrPc on the WSe_2 FET. Three consecutive measurements are shown for both *off*- and *on*-state. The CoCrPc itself shows some degree of bistability, and it the characteristics are repeatable. **(c)** Programming tests after adding

$LiClO_4$ to the CoCrPc. The magnitude of threshold voltage shift increases significantly, indicating an increase in the channel doping. **(d)** Programming tests after adding the h-BN capping layer on top of the monolayer electrolyte on the FET. The threshold voltage shift increases, particularly for the *off*-state.

To quantify the shifts in the transfer curves after programming, we track the V_s, defined as the smallest voltage within the subthreshold swing (SS) region over two decades of current (**Figure S8)**. The charge induced after programming (ΔQ) is estimated as $\Delta Q = C_{ox} \Delta V_{th}$, where C_{ox} is the capacitance of the back-gate dielectric SiO_2 (38.37×10^{-9} F cm^{-2} for 90 nm of SiO_2). The corresponding change in sheet charge carrier density (n_s) is calculated by $n_s = \Delta Q/e$, where e is the charge of a single electron. These values are tabulated in **Table S2**.

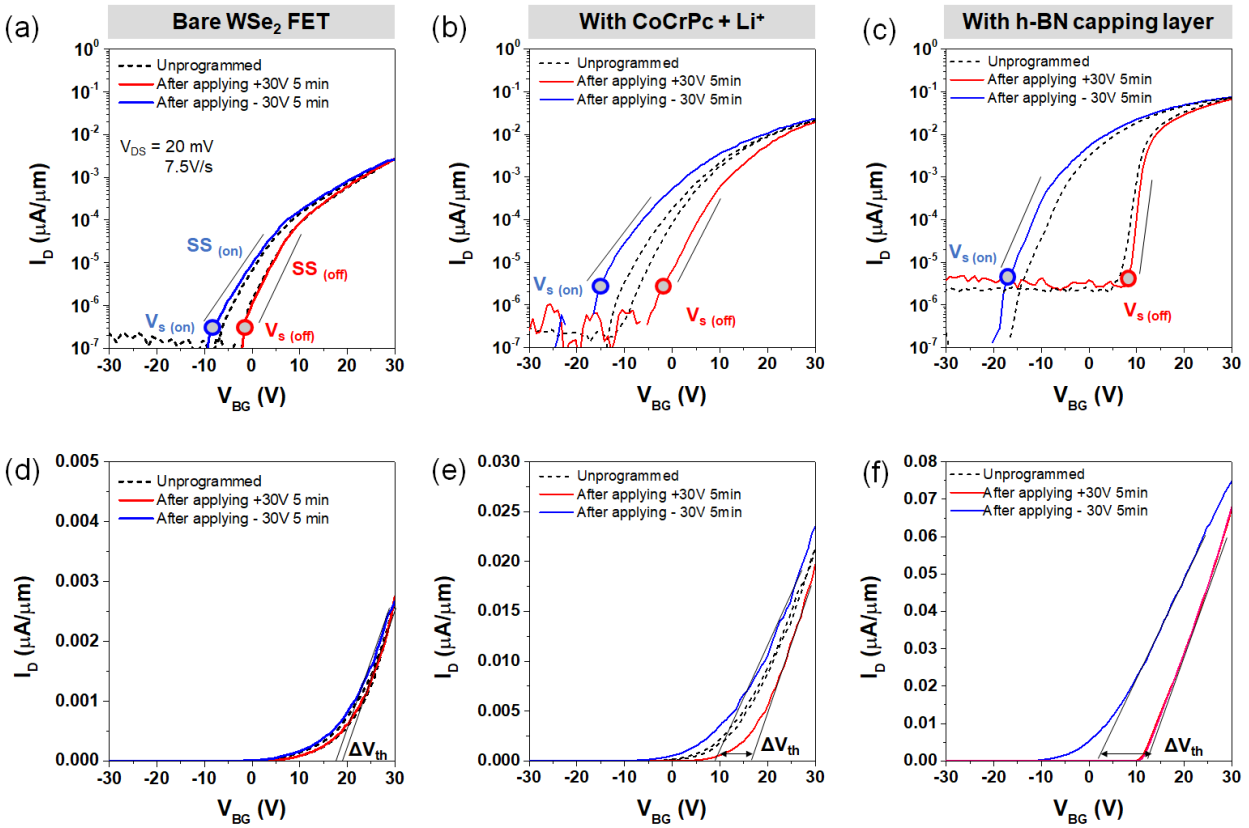

Figure S8. The subthreshold swing and the V_s for the *on*- and *off*-state after programming. The transfer curves for the bare WSe_2 FET, after adding CoCrPc + Li^+ and after adding h-BN are shown in **(a)** – **(c)** in a log y-axis scale, with the black solid lines indicating the range over which the subthreshold swing is calculated (i.e., at least two decades of current). The minimum voltage of the SS range is defined as V_s to quantify the *on*- and *off*-states after programming the device. The transfer curves are repeated in **(d)** – **(f)** on a linear scale, with the threshold voltage shift (ΔV_{th}) shown for each.

Table S2. Summary of transfer characteristics of the WSe_2 FET.

WSe_2 FET	SS (off) [V/dec]	SS (on) [V/dec]	V_s (off) [V]	V_s (on) [V]	V_s shift ΔV_{th} [V]	V_{th} after *off*-programming [V]	V_{th} after *on*-programming [V]	Threshold voltage shift ΔV_{th} [V]	Charge density change n_s [cm^{-2}]	Drain current I_D ratio at V_{BG} = 0 V
Bare	3.1	5.5	- 2.3	- 8.3	6.0	+ 19.1	+ 17.3	1.8	4.3×10^{11}	11.6
Add CoCrPc + Li^+	4.5	4.8	- 2.0	- 16.2	14.2	+ 16.5	+ 8.9	7.6	1.8×10^{12}	84.4
Add h-BN capping layer	1.0	3.6	+ 9.0	- 18.0	27.0	+ 12.6	+ 2.1	10.5	2.5×10^{12}	2.2×10^4

Part 7. Programming tests

The programming tests were designed to *modulate* the state of the monolayer electrolyte during the 5-min programming time with a constant back gate voltage, and then to *sense* the state as a result of programing using a fast single sweep (7.5 V/s). The direction of transfer scan is designed to be in accordance with the polarity of previous programming to minimize the possibility of altering the state during the sense process.[7] For example, after programming at +30 V, the transfer curve is measured from +30 to -30 V. In this way, the reverse programming of the device is minimized during the transfer measurement. In addition, at the beginning of a programming test series (before a programming voltage is applied), we took a fast (7.5 V/s) *double* sweep transfer scan to *sense* the state(s) of device in an unprogrammed condition.

For example, as shown above in Figure S8 (b), for the MERAMs without h-BN, a fast double sweep transfer scan was taken before the programing tests, which showed a small shift of V_s that is likely caused by charge trapping and detrapping at the WSe_2/SiO_2 interface.[8,9] Note that we observed identical small shifts of V_s on the bare WSe_2 FETs (Figure S8 (a)). After the programming tests, we clearly sense the two states of the monolayer electrolyte, which are indicated by the two transfer curves with large shift (ΔV_s). The transfer measurements themselves do not program the device, and this is backed-up by two pieces of evidence on the MERAM without h-BN: 1) the initial double sweep transfer scans are similar to the bare FETs, and 2) the Vs shift is much larger for the transfer curves after programming than the initial double sweep for unprogrammed devices. These observations are in accordance with previous results on graphene FETs.[7]

In contrast, for the MERAM for which h-BN has been added, the initial double sweep transfer scans exhibit an increased V_s shift compared to the bare FETs. More specifically, the magnitude of the V_s shifts is comparable to those observed during programming (black dash in Figure S8 (c)). Thus, in contrast to the devices without h-BH, the state of the monolayer electrolyte was switched during the transfer scans, which could possibly be explained by h-BN reducing the energy barrier to switching. To investigate the minimum voltage required to switch the device, we monitored the *on/off* ratio of two states while varying the V_{BG} (see Figure S12 (Device 2)). Using a programing voltage of ~ ± 20 V and a programing time of one-second, we can switch the states of the monolayer electrolyte with an *on/off* ratio of ~ 10^4. This finding agrees with our observation in the programming test transfer measurements and supports the conclusion that the device with h-BN was switched *during* the transfer scans of -30 to 30 V and then back to -30V. The reason that the transfer curves do not overlap above the measured minimal switching voltage (~20 V) can likely be attributed to intrinsic hysteresis caused by charge trapping (Figure S8 (c)).

Because of the bistability of MERAM, the hysteresis window is expected to be a function of the sweep rate. Thus, double transfer scans were measured at sweep rates varying from ~ 100 mV/s to 10 V/s on an unprogrammed, newly fabricated MERAM (Device 3). **Figure S9** shows that the hysteresis increases with decreasing sweep rate as more time is provided for the ions to switch. This result agrees with our previous observation on monolayer electrolyte graphene FETs.[6] Note that this trend is the opposite of the trend for ion-gated FETs without bistability where hysteresis *decreases* with decreasing sweep rate.

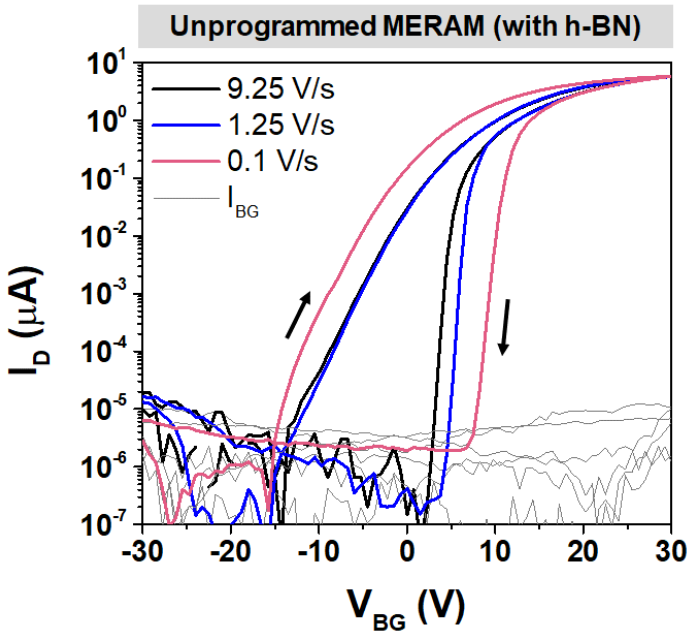

Figure S9. Double-sweep transfer characteristics of an unprogrammed MERAM (Device 3) as a function of sweep rate. The scans were taken from negative to positive V_{BG} and back with the sweep rates of 9.25 (black), 1.25 (blue) and 0.1 V/s (red). V_{DS} = 100 mV.

Part 8. Bistability of the monolayer electrolyte on MoS_2 FETs

The bistability of monolayer electrolyte has been also observed on other 2D MERAMs. For example, the monolayer electrolyte was deposited and on back-gated MoS_2 FETs (**Figure S10** (a) – (c)) and the electrical measurements (Figure S10 (d)) indicate a similar shift of V_s after programming *on*/*off*, indicating the bistability.

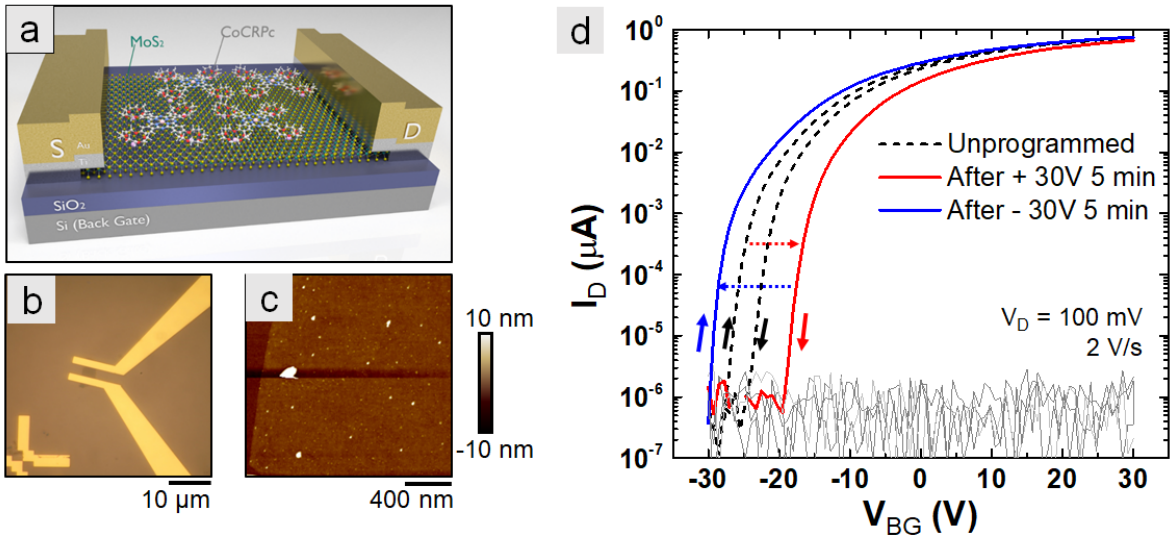

Figure S10. Backgated MoS_2 MERAM. (a) Device schematic of a backgated MoS_2 FET with the monolayer electrolyte. **(b)** Optical image of a device. **(c)** AFM scan of a MoS_2 channel with the monolayer electrolyte; the white particles are CoCrPc aggregates. **(d)** Transfer characteristics before (black dash) and after programming *off* (red line) and *on* (blue line).

Part 9. Program/erase on a backgated WSe_2 FET with only the monolayer electrolyte (no h-BN)

Figure S11 shows the endurance (a) and retention test (b) on a MERAM without h-BN capping. Two distinct states are observed during 1000 cycles of program/erase and each state can be maintained over six hours, but with a smaller *on/off* ratio (~ 1.3) compared to the devices capped with h-BN.

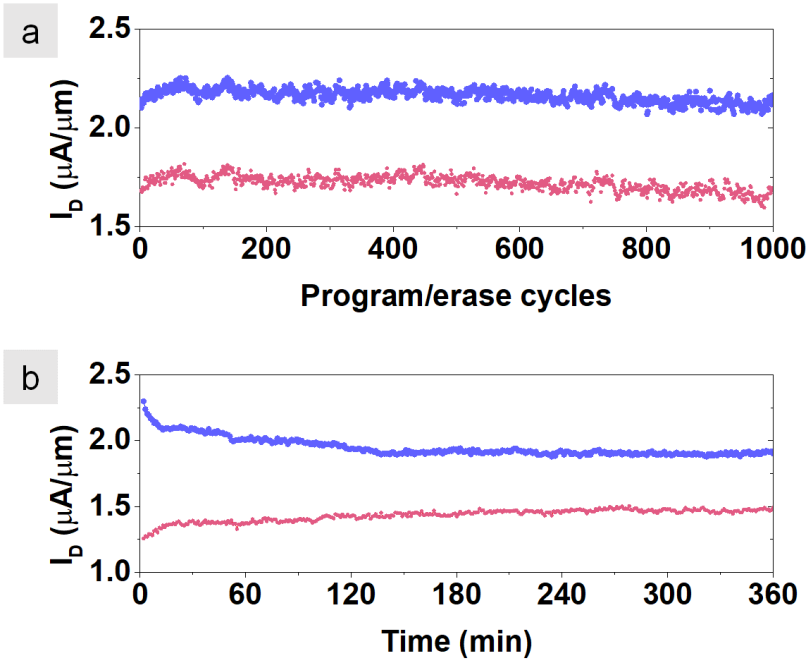

Figure S11. Program/erase tests using V_{BG} on a backgated WSe_2 FET with only monolayer electrolyte (no h-BN). (a) Program/erase endurance test. 1000 cycles of program/erase with pulse with of 1 s, readout time of 10 s, and V_{DS} = 500 mV. **(b)** Retention test. Program/erase with 60 s pulse and I_D monitored for 6 hours. High/low current states are in blue/red color, respectively.

Part 10. Program/erase measurements as a function of back gate voltage on two MERAMs (with h-BN)

In **Figure S12**, the *on*- and *off*-states are monitored while varying the $|V_{BG}|$ during program/erase (negative/positive V_{BG}) for 2 MERAMs. Note that the minimum V_{BG} required to fully switch the MERAM from one state to the other is different on two MERAMs, which could be due to the differences in field screening resulting from varying WSe_2 channel thicknesses (~ 8 nm for Device 1, 6 nm for Device 2).

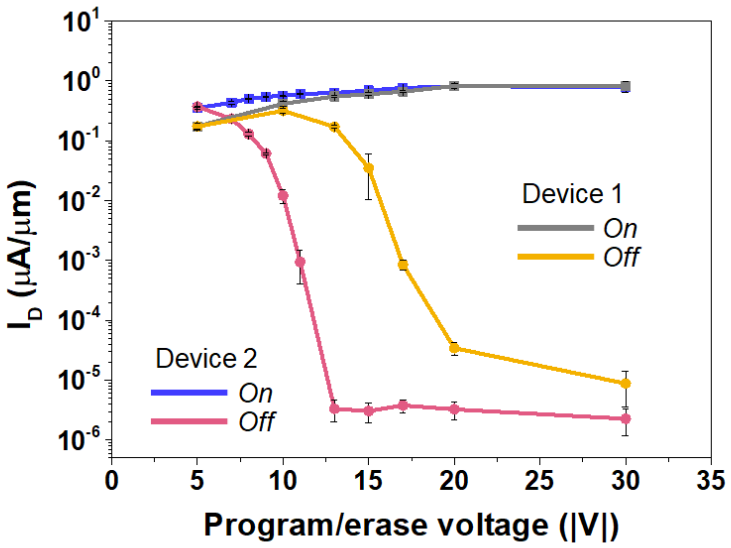

Figure S12. Program/erase tests using different V_{BG} on two MERAMs. The program and erase voltages vary from ± 5 to ± 30 V. The pulse width is 1 second and the readout is 10 seconds at V_{BG} = 0 V; V_{DS} = 500 mV. Data at each point are averaged over 12 program/erase cycles with the error bar indicating one standard deviation from the mean.

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