SUPPORTING INFORMATION

Electroforming-free Bipolar Resistive Switching in GeSe Thin Films with a Ti-containing Electrode

Woohyun Kim, Chanyoung Yoo, Eui-Sang Park, Manick Ha, Jeong Woo Jeon, Gil Seop Kim,

Kyung Seok Woo, Yoon Kyeung Lee[*]*, and Cheol Seong Hwang*[*]

Department of Materials Science and Engineering and Inter-University Semiconductor Research Center, College of Engineering, Seoul National University, Seoul 08826, Republic of Korea

*E-mail: (Y.K.L) greense9@snu.ac.kr, (C.S.H) cheolsh@snu.ac.kr

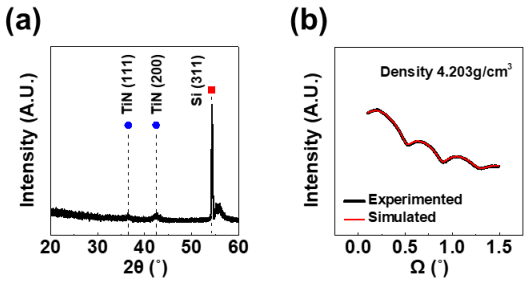

Figure S1. (a) GAXRD patterns of the as-deposited GeSe films on the TiN substrate through ALD-DFM. (b) XRR results for the GeSe films.

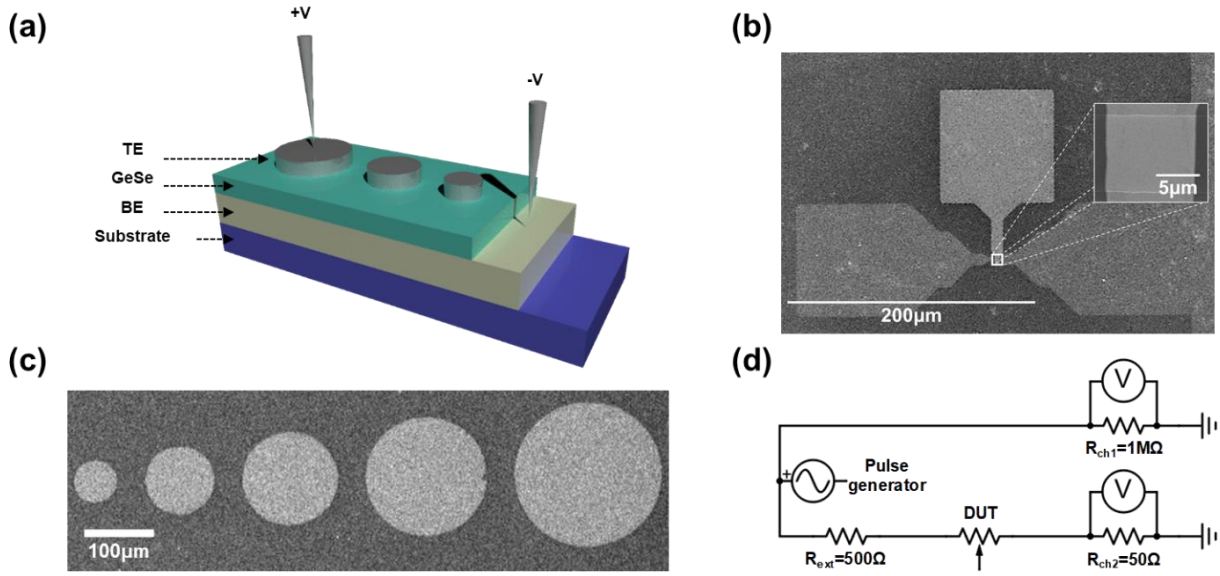

Figure S2. (a) Schematic diagram of the vertical structure of the fabricated devices and measurement setup. The top-view SEM image of devices in (b) a crossbar-type and (c) dot-patterned structure. (d) Experimental set-up for the time-resolved pulse measurement.

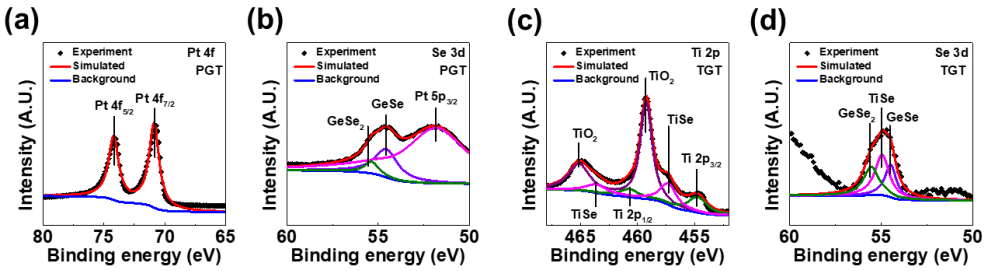

Figure S3. XPS results of (a,b) PGT and (c,d) TGT (Ti/GeSe/TiN) layers with thin top metal layer (~5nm) without Ar^+ sputtering. The deconvoluted TiSe peak in Figure S3(c) denotes that the interfacial Ti-Se layer was not formed by Ar^+ sputtering. The difference in the relative intensities of the peaks compared to the etched samples (Figure 1(c)) is originated from the higher susceptibility to surface oxidation of Ti under the air exposure without a Pt capping layer.

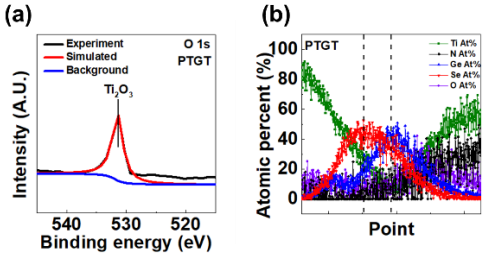

Figure S4. (a) XPS results and deconvoluted peak of O for PTGT layers. (b) EDS analysis of PTGT layer with O At%.

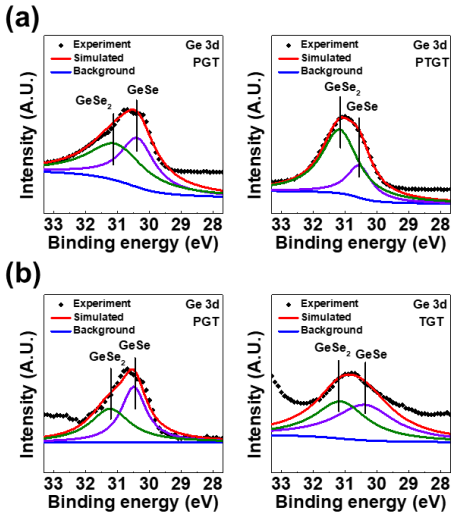

Figure S5. XPS results of the (left) Pt/GeSe interface and (right) Ti/GeSe interface (a) with and (b) without Ar^+ sputtering.

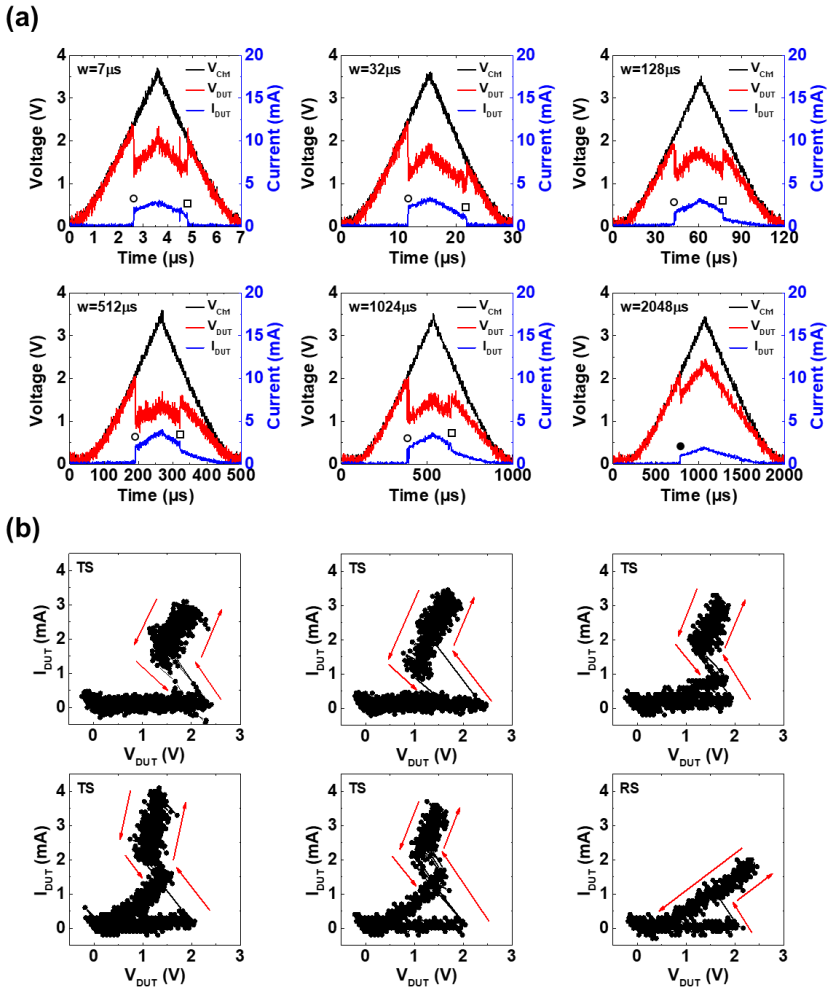

Figure S6. (a) Time-resolved measurement of PGT crossbar-type devices with different pulse widths (w). (b) I-V curve converted from V-t curve. In Figure S6(a), the black lines represent the applied voltage measured at channel 1 (Ch1 in Figure S2(d)), and the red and blue lines represent the voltage and current across the device under test (DUT), respectively. It was seen that the PGT sample showed a sudden increase in device current (I_{DUT}) at a certain time during the pulse increase (the open-circle symbol in the left panel of Figure S6(a)), which corresponds to TS-on, whereas the increased I_{DUT} suddenly decreased at a certain time during the pulse decrease, which corresponds to TS-off (the open-square symbol in the left panel of Figure S6(a)), at the w of 7 to 1024 µs.

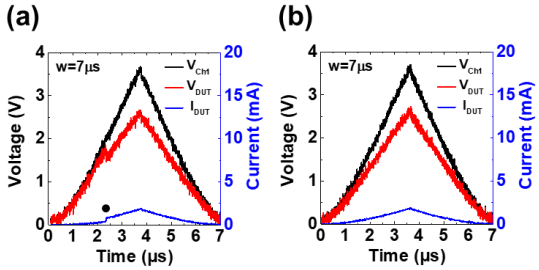

Figure S7. Time-resolved measurement of PTGT crossbar-type devices with w=7μs showing only (a) RS behavior and (b) LRS after the SET operation.

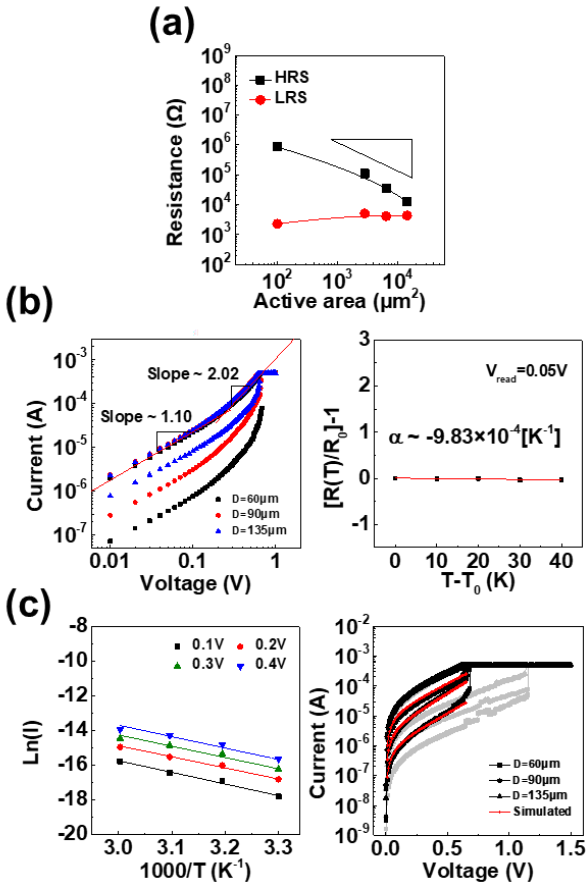

Figure S8. Conduction mechanism of PGT device. (a) Summary of area dependency of resistance. (b, left) logI-logV curves in the DC sweep. (b, right) Temperature dependence of the LRS resistance. (c) HRS conduction. (c, left) LnI as a function of the inverse temperature. (c, right) LogI-V curves of HRS in the DC sweep and its fitting to a modified Poole-Frenkel conduction mechanism.

The PGT device exhibited the area-independent CF behavior identical to the PTGT device in Figure S8(a). Two regions with different LRS slopes (1.10 and 2.02) were observed in Figure S8(b, left), indicating the space charge limited conduction (SCLC) mechanism. Figure S8(b, right) shows the variation of the reduced LRS resistance (normalized to the value at room temperature) as a function of the measurement temperature. The slope of the best-linear-fitted graph corresponds to the temperature coefficient of resistance (TCR), and it was ~-9.8x10^{-4}, indicating the highly disordered semiconducting behavior of the CF in the PGT device. This finding is consistent with the conception that the CF in the PGT device must be composed of heavily Se-deficient Ge_xSe_{1-x} (or even defective Ge clusters), which may have a high density of trap levels in its band gap. The conduction of the HRS region was not different from the PTGT device.

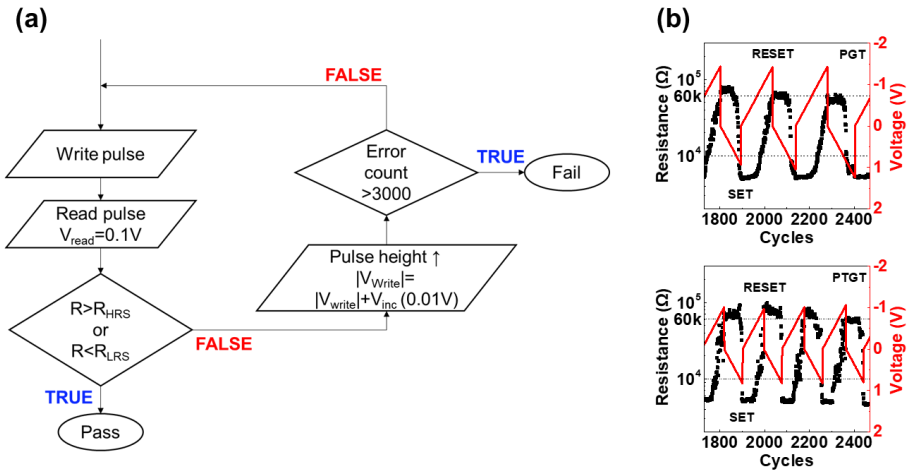

Figure S9. (a) Schematic flowchart of the in-house-built CLPS measurement. The amplitude of write pulse is increased until the target resistance is achieved. (b) The results with HRS>60 kΩ, LRS<10 kΩ in PGT device (b, upper) and PTGT device (b, bottom). The voltage (red line) is linearly increased until the resistance (black dots) reaches the target value (horizontal dashed lines).

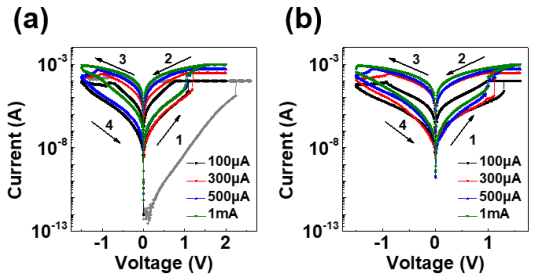

Figure S10. BRS I-V characteristics of the (a) PGT requiring forming process, (b) PTGT forming-free devices fabricated in crossbar-type devices.

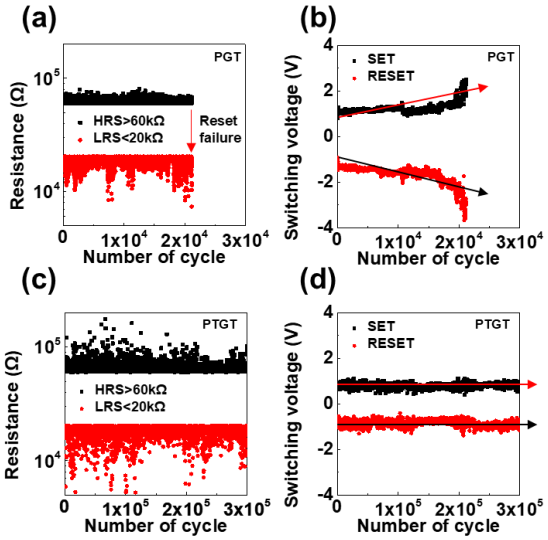

Figure S11. Variations in the LRS/HRS resistance in CLPS cycling and switching voltages of devices required to achieve with the setting values of HRS > 60kΩ, LRS < 20kΩ. (a,b) PGT devices. (c,d) PTGT devices.

Fitting parameter	Diameter [μm]		
	60	90	135
Inter-trap distance [nm]	4.34	4.85	4.80
Trap density [cm^{-3}]	2.53×10^{19}	2.25×10^{19}	1.80×10^{19}

Table S1. Trap density (N_T) and inter-trap distance (Δz) calculated by fitting the I-V curve to the modified Poole-Frenkel conduction equation.