Supporting information for

Vertically Stacked CVD-Grown 2D Heterostructure for Wafer-Scale Electronics

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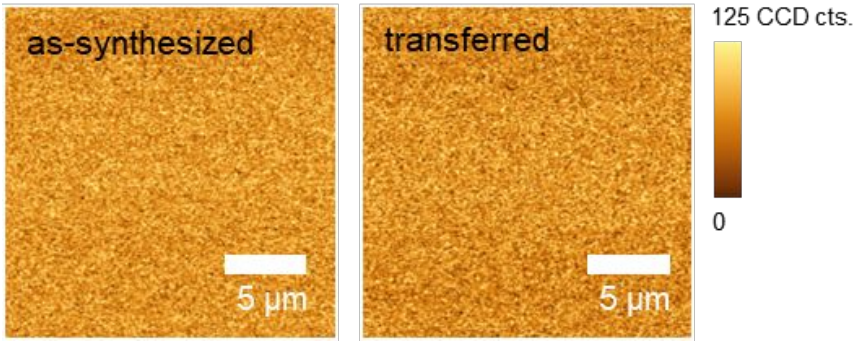

Figure S1. Raman mapping images of as-synthesized and transferred bulk MoS_2 by E^1_{2g} mode frequency.

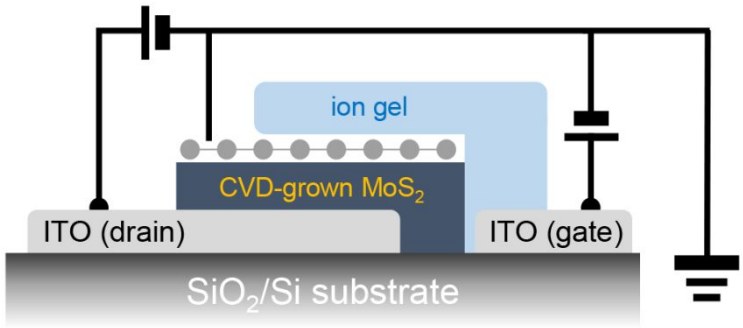

Figure S2. Cross-sectional schematic structure of the vertical transistor.

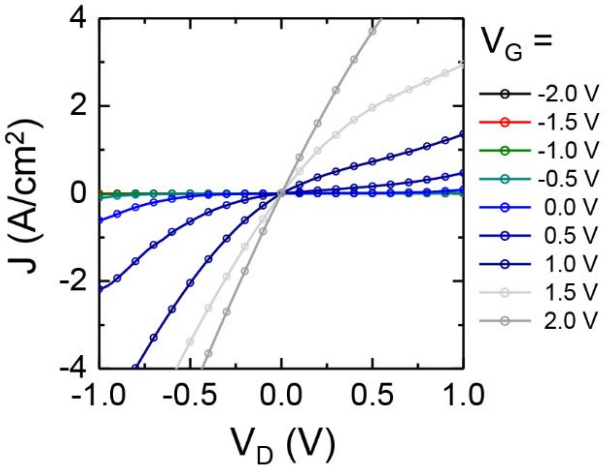

Figure S3. Linear plot of output characteristics of the vertical transistors at different V_Gs.

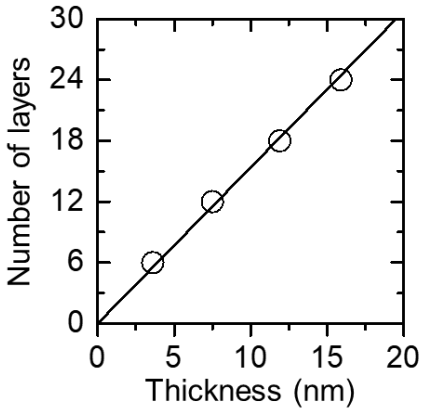

Figure S4. Number of MoS_2 layer as a function of the thickness.

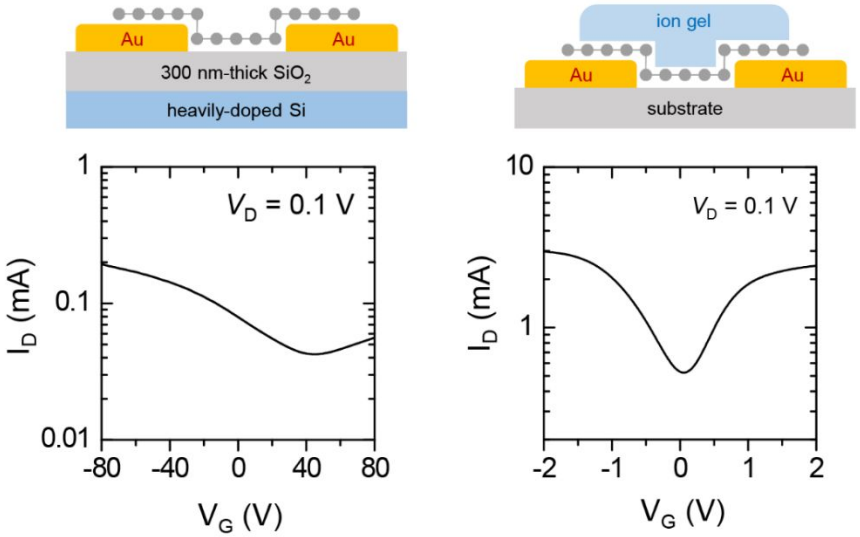

Figure S5. Transfer characteristics of the graphene transistors with the SiO_2 back gate dielectrics and the ion gel top-gate dielectrics.

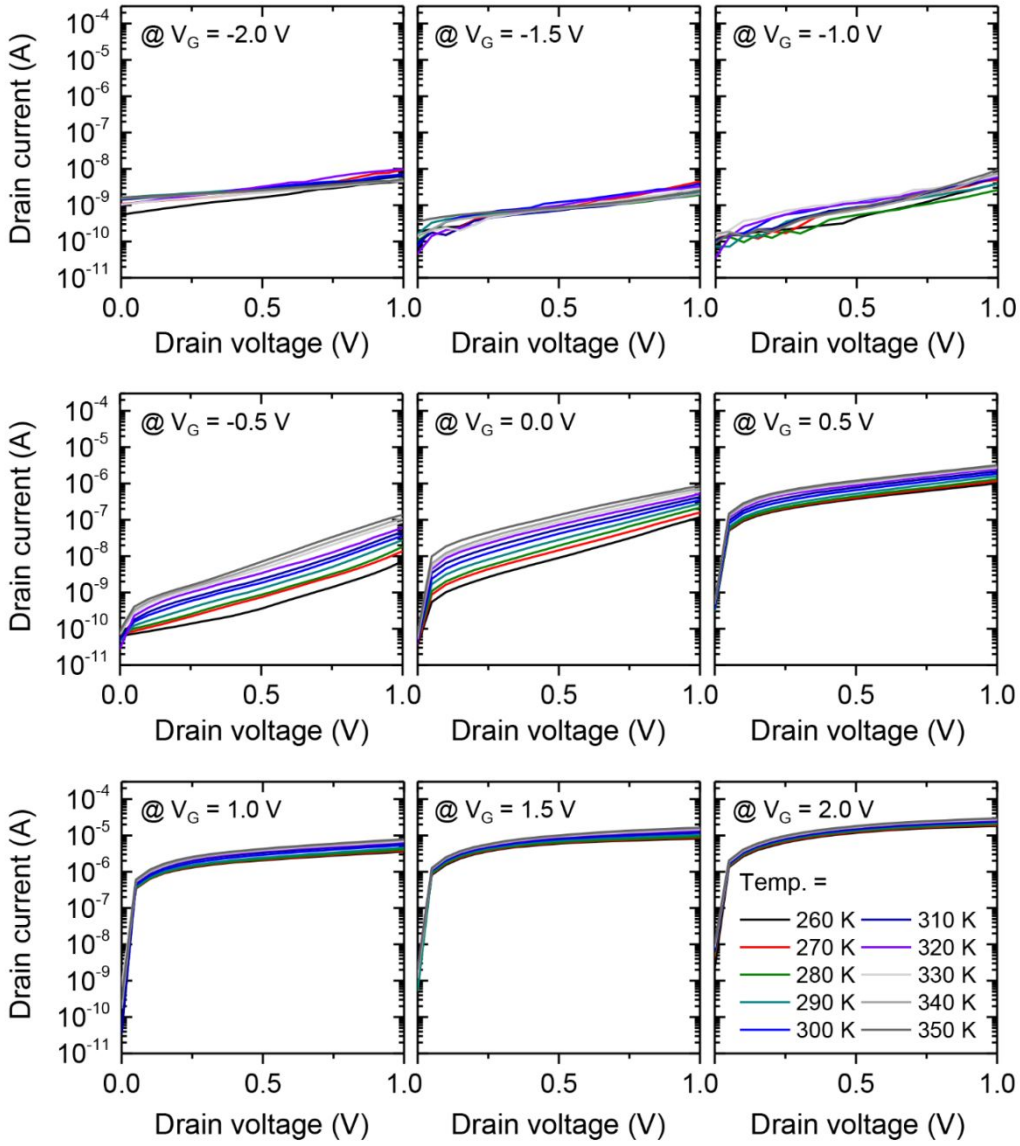

Figure S6. Output characteristics of the vertical transistors measured under various temperatures and V_Gs.

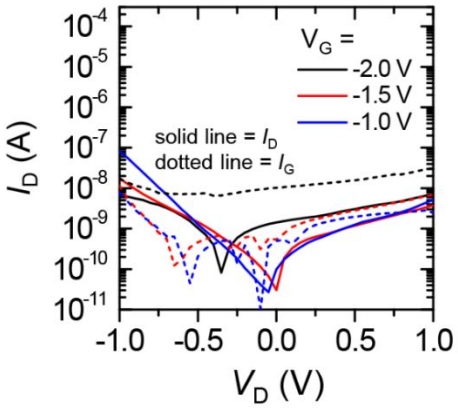

Figure S7. I_D and I_G as a function of V_D of the vertical transistors at V_G = -1.0, -1.5, and -2.0 V.