

Supporting Information

Ferroelectric second-order memristor

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S1 SAMPLE FABRICATION

Hf_{0.5}Zr_{0.5}O₂ (HZO) film 4 nm in thickness was grown by ALD technique (ALD reactor Sunale R-100 Picosun OY) at $T = 240^{\circ}\text{C}$ on highly doped (100) p⁺-Si substrate ($\rho = 0.005 \text{ } \Omega\cdot\text{cm}$) using Hf[N(CH₃)(C₂H₅)₃]₄ (TEMAH), Zr[N(CH₃)(C₂H₅)₃]₄ (TEMAZ) and H₂O as precursors and N₂ as carrier and purging gas. Initial native SiO₂ layer was removed by 1% HF buffer solution and then repeatedly grown at standard conditions in order to exclude the influence of the prior wet cleaning procedure.

Top TiN electrode 20 nm in thickness was further deposited by magnetron sputtering from Ti target in N₂ and Ar ambient (1:10) at 250°C. Rapid thermal annealing ($T = 500^{\circ}\text{C}$, 30 s) in Ar atmosphere was further used yielding the crystallization of the underlying HZO films.

Patterning of the circular top electrodes was further performed using maskless optical lithography (Heidelberg Instruments MLA 100) and plasma chemical etching in SF₆. To improve the endurance of the ferroelectric capacitors (FE) under investigation an additional Al layer 200 nm in thickness was deposited on top of TiN electrodes using e-beam evaporation and standard lift-off procedure. Photoresist mask for lift-off procedure was prepared by maskless optical lithography (Heidelberg Instruments MLA 100). The electrical contact to the bottom p⁺-Si electrode was made as a macro-size contact pad.

S2 TRANSMISSION ELECTRON MICROSCOPY

Transmission electron microscopy (TEM) cross-sections of both as-grown amorphous and crystallized cycled HZO film were prepared with focused ion beam milling in JIB-4501 MultiBeam SEM-FIB (Jeol). TEM study was conducted with JEM-2100 (Jeol) transmission electron microscope operating at the accelerating voltage 200 kV.

TEM analysis of non-annealed p⁺-Si/HZO sample cross section reveals the presence of native SiO_x interlayer ~ 1 nm in thickness and amorphous state of 4-nm-thick HZO film (Figure S1a). The annealed p⁺-Si/HZO/TiN stack comprises polycrystalline HZO film (Figure S1b). The SiO_x interlayer has not increased in thickness during the annealing (Figure S1b).

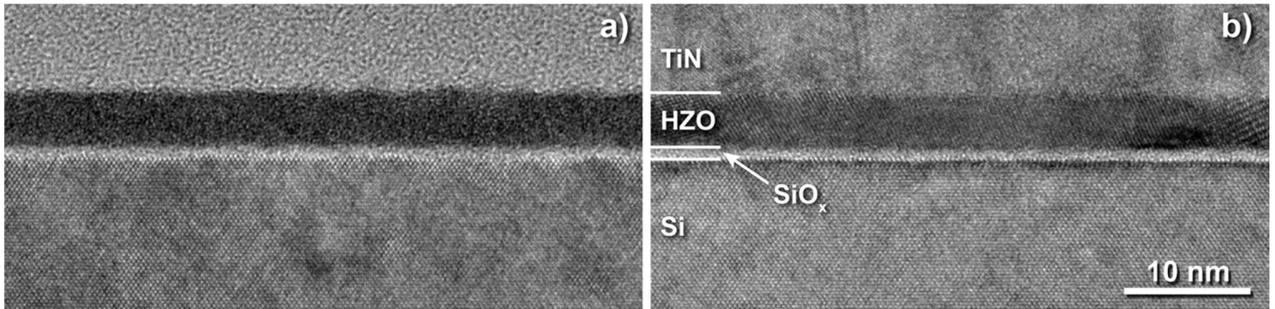


Figure S1. TEM images of as grown p⁺-Si/HZO (a) and annealed p⁺-Si/HZO/TiN (b) structures cross sections

S3 FERROELECTRIC CHARACTERIZATION

Ferroelectric response of the p⁺-Si/HZO/TiN capacitor was studied by PUND technique (Positive Up Negative Down) using Cascade Summit 1100 probe station coupled with Agilent semiconductor device analyzer B1500A containing two B1530A waveform generator/fast measurement units and two source/measurement units connected via a selector. The bottom electrode was grounded, whereas the bias voltage was applied to the top electrode.

Typical voltage pulse set and current signals are shown in Figure S2. An input pulse set consists of two pairs of identical unipolar (positive and negative) triangular pulses. During the first pulse in the

pair the current I_{sw} is the sum of the current associated with the switching of polarization plus both the leakage and the capacitive displacement current, while the current during the second pulse I_{non-sw} has only non-polarization switching contributions and originates from the leakage and the capacitive displacement current. The polarization switching current can be found as a difference between the integral current signals generated by the first and second unipolar pulses.

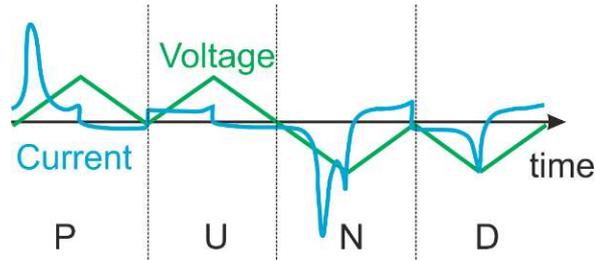


Figure S2. A typical PUND voltage pulses used for the pulsed switching testing and the sketch of transient currents

In this work, the switching polarization value was measured using the voltage sweep with the positive/negative pulse amplitude +4 V/-3 V and pulse duration 10 μ s.

S4 R_{OFF}/R_{ON} RATIO MEASUREMENTS

Measurement of R_{off}/R_{on} ratio was performed using staircase sweep dc $I-V$ measurements. The bottom Si electrode was grounded, whereas the switching voltage was applied to the top TiN electrode.

The internal built-in electric field in the studied devices results in the instability of the downward polarization. In order to maintain unstable polarization direction after the switching, one has to apply an external electric field, which is large enough to compensate for the internal depolarization field. For this purpose, the measurements of R_{OFF}/R_{ON} ratio were performed using the staircase dc $I-V$ sweeps (Figure S3). The voltage applied to the top electrode maintained constant during the current measurements. The voltage increment is performed without passing through zero and thus, after the

polarization reversal into unstable downward direction under sufficient electric field no depolarization effect occurs until the built-in electric field exceeds the coercive voltage.

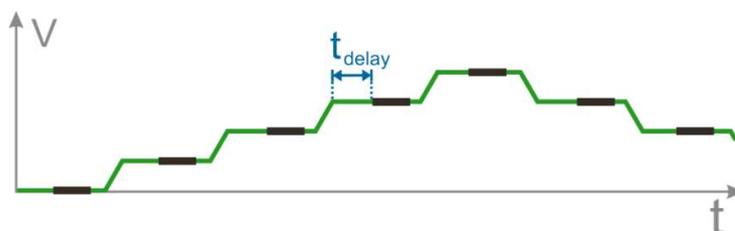


Figure S3. Voltage profile (green) applied to a structure during *dc I-V* measurements. Black lines demonstrate time intervals during which the current across the structure is being measured

One has to choose the proper delay time between last voltage shift and the beginning of the current measurement (t_{delay} in Figure S3). The voltage change induces significant capacitive current, which may give a contribution to the measured current if the time delay is small. Small delay would result in *I-V* curve zero offset. It is worth to mention that the contribution of the capacitive current can be estimated as the current near zero voltage. In addition, on presented *I-V* curves the capacitive current was more than 100 times smaller than the switching currents.

The differential resistance values were calculated in a conventional way, i.e., as a ratio of the current increment on the voltage difference at the read voltage.

The electrical cycling leads to the evolution of static *I-V* curves. The *I-V* loop becomes more open and wider, presumably, following the opening of the initially pinched *P-V* hysteresis (Figure S4). As a result, the $R_{\text{OFF}}/R_{\text{ON}}$ ratio increases. In addition, the current measured at readout voltage increases during the bipolar electrical cycling both at OFF and ON states. The increase in leakage current during the electrical cycling is usually explained by the generation of the oxygen vacancies.¹

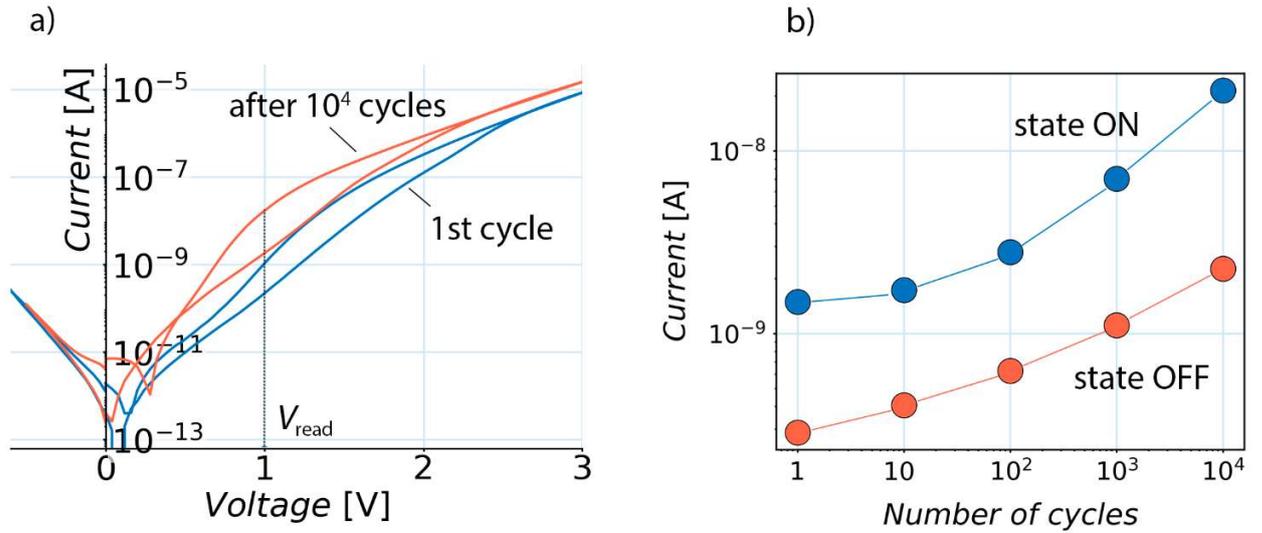


Figure S4. a) Static I - V curves at the first cycle and after 10^4 cycles;
b) Evolution of the current at ON and OFF state during electrical cycling (at $V_{\text{read}} = 1$ V)

S5 CAPACITANCE-VOLTAGE MEASUREMENTS

Capacitance-voltage (C - V) curves acquired on the metal-oxide-semiconductor (MOS) structure strongly depend on Si dopant concentration and the thickness of oxide dielectric layer. In case of high dopant concentration in semiconductor and thin oxide layer, the inversion capacitance value is close to maximum for MOS structure oxide capacitance(1).² Once p^+ -Si is used as a bottom electrode in a compartment with thin dielectric layer, C - V measurements are difficult due to the similarity of the inversion capacitance and the oxide capacitance values. For this reason, additional (100) p-Si ($\rho = 10 \text{ Ohm}\cdot\text{cm}$)/HZO/TiN structures were fabricated for the C - V measurements using the same procedure as described in Section S1.

C - V curves were acquired using Cascade Summit 1100 probe station coupled with Agilent semiconductor device analyzer B1500A containing LCR meter. Probe voltage with 50 mV amplitude and 1 MGz frequency was used during measurements. The obtained impedance data were processed using series capacitance model (C_s - R_s).

The measured C - V curve for p-Si/HZO/TiN structure 50 μm in diameter is presented in Figure S5. The observed hysteresis should be apparently attributed to the charging of interface states adjacent to Si. The maximal capacitance equal to the net HZO capacitance (C_{ins}) reaches $\sim 6.7 \cdot 10^{-11}$ F, which corresponds to the effective $k_{\text{HZO}} \sim 19$.

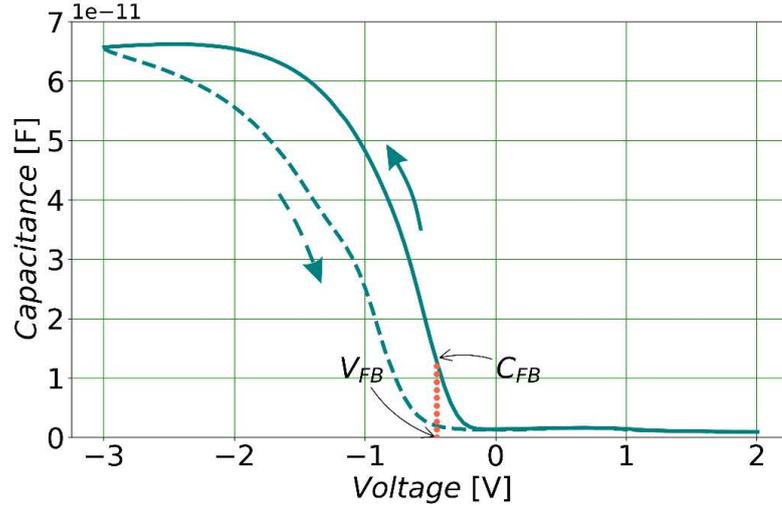


Figure S5. Capacitance-voltage curve of p-Si/HZO/TiN structure

The flat band capacitance (C_{FB}) might be estimated using the following expression³:

$$C_{\text{FB}} = C_{\text{ins}} \frac{k_{\text{ins}}}{d + (k_{\text{ins}}/k_s)L_D}, \quad (1)$$

where k_{ins} and k_s are the permittivity of insulator and semiconductor, respectively, L_D is a Debye length in the semiconductor.

For dopant concentration 10^{17} cm^{-3} , $C_{\text{FB}}/C_{\text{ins}}$ value reaches ~ 0.2 corresponding to the flat band voltage -0.45 V.

Both the presence of hysteresis and the negative flat-band voltage indicates the presence of positive charge (dopant-type defect states) at the interface with the semiconductor.

S6 ENERGY BAND DIAGRAM SIMULATIONS

Energy band diagram simulations were performed by the finite element modelling using Comsol software and built-in semiconductor physics model in 1D geometry. Usually, MOS structure can be simulated using thin insulator gate domain (here and further, we use the terms of Comsol software). In the case of ferroelectric layer, the polarization charge is located at the same interface, where this domain was used. The voltage dropped across a dielectric can be calculated as the voltage difference between the applied voltage and the voltage probed at Si/dielectric interface.

Considering both $C-V$ and $I-V$ data, we assume that in quasistatic case the depolarization field is attributed to the built-in charge close to Si/HZO interface. Therefore, one has to set an additional surface charge so that the simulated potential at Si/dielectric interface at zero voltage would be equal to the flat band voltage $V_{\text{FB}} = -0.45$ V derived from $C-V$ data. Such additional surface charge was found to be $\sim 1 \mu\text{C}/\text{cm}^2$, which corresponds to the trap density of $\sim 7 \cdot 10^{12} \text{ cm}^{-2}$. In simulation, we assume that additional interface charge does not depend on voltage applied to the structure.

The polarization surface charge was estimated using an additional condition. Namely, PUND measurements yield the coercive electric field for such films 1.1 MV/cm. Therefore, one has to set the polarization charge value so that the electric field in dielectric would reach 1.1 MV/cm at external voltages equal to observed from measured coercive voltages. Simulated electric field in ferroelectric for two different polarization directions with polarization charge equal to $1.6 \mu\text{C}/\text{cm}^2$ as a function of external voltage is presented in Figure S6. It is clearly seen, that coercive voltages derived from Figure S6 is close to coercive voltage obtained from Figure 2. The simulation parameters are collected in Table S1.

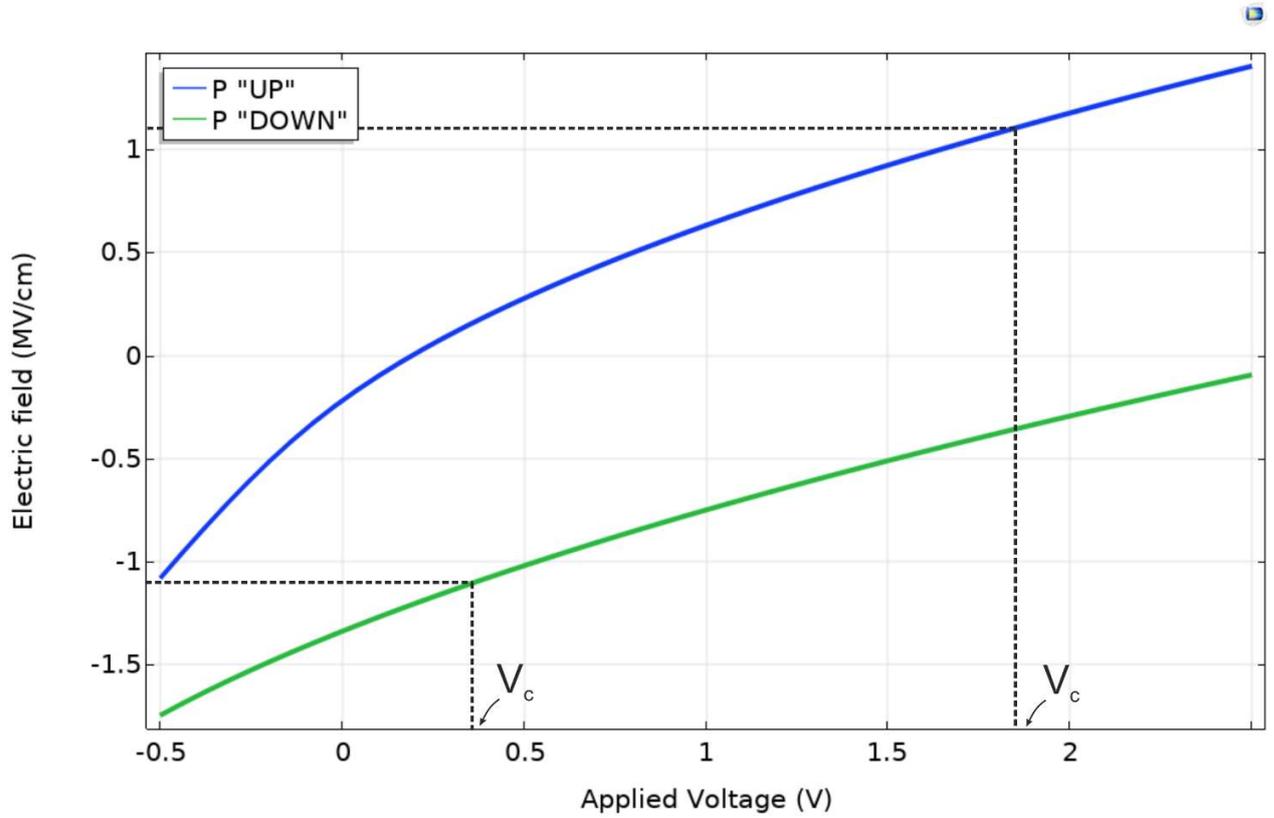


Figure S6. Simulated electric field in ferroelectric as a function of applied voltage for different polarization directions. Coercive voltages (V_c) correspond to coercive electric field for such films (1.1 MV/cm)

Table S1. Simulation parameters

Parameter	Value
Acceptor doping concentration	$2 \cdot 10^{19} \text{ cm}^{-3}$
TiN work function	4.7 eV
Additional surface charge	$1 \mu\text{C}/\text{cm}^2$
Polarization charge	$\pm 1.6 \mu\text{C}/\text{cm}^2$
HZO relative permittivity	20

S7 HARD X-RAY PHOTOEMISSION SPECTROSCOPY MEASUREMENTS AND ANALYSIS

HAXPES measurements on the p^+ -Si/HZO/TiN structures were performed at the beamline P22 of PETRA III (DESY) with Specs 225 HV analyzer choosing an excitation energy $E = 6$ keV with an overall energy resolution of about 0.2 eV.⁴ The regions of interest Hf4*f* and Si2*p* were acquired at the glancing angle 5° with normal photoelectron takeoff. The Hf4*f* and Si2*p* core-level spectra acquired during HAXPES analysis from the p^+ -Si/HZO/TiN structure are given in Figure S7.

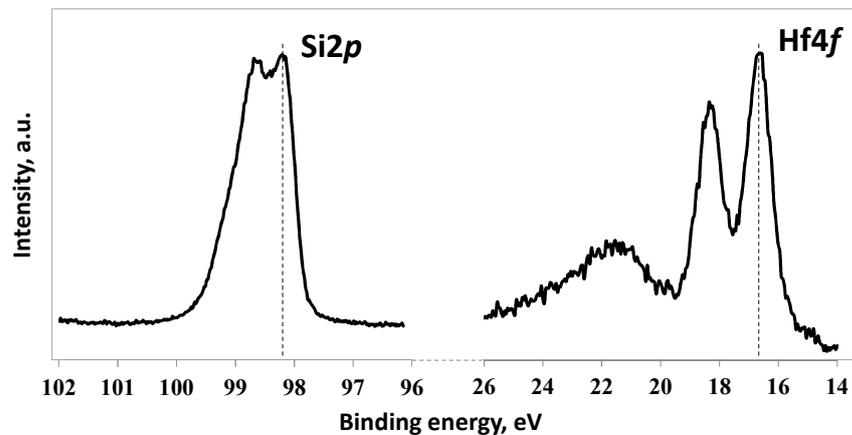


Figure S7. Hf4*f* and Si2*p* core-level spectra taken from p^+ -Si/HZO/TiN structure

The electrical potential distribution in Si close to the top interface results in the shift and broadening of the core-level lines spectra. Thus, the potential profile can be reconstructed from the collected spectra utilizing the following methodology.

Each Si2*p* spectrum taken from the p^+ -Si/HZO/TiN sample was simulated as a sum of several components (~ 200 in our case), representing virtual sub-layers equally distributed within the depth range 0-30 nm adjacent to Si/HZO interface. This depth was chosen to cover the 3λ range (where λ is the effective attenuation length of photoelectrons for these kinetic energies), from which $> 99\%$ of collected photoelectrons are coming. Each component has its own binding energy shift proportional

to the potential at the particular depth z , and its intensity is given by $I_{e^-} = I_{h\nu}(z) \cdot q \cdot e^{-z/\lambda}$, where $I_{h\nu}(z)$ is X-ray intensity at the depth z , q - the photoionization cross-section (Figure S8).

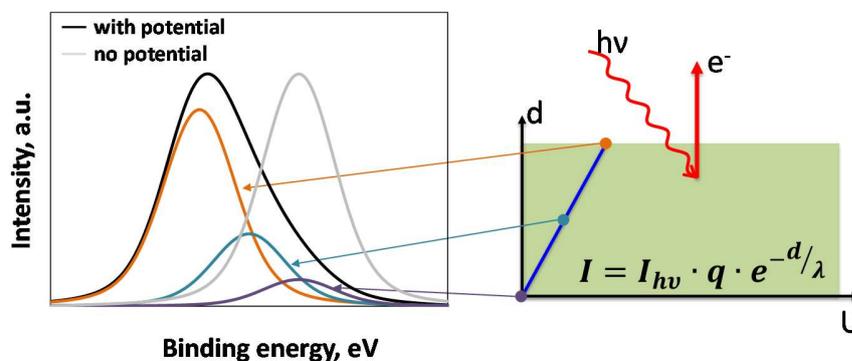


Figure S8. The schematic illustration of the core level spectra broadening arising from the distribution of the potential across and photoelectrons intensity attenuation in the layer

The shape of individual component was taken from the reference pure p^+ -Si sample, where there is no electrical potential distribution. In order to regularize the fit, we assumed the quadratic potential drop in Si, which represents the band bending of uniformly doped semiconductor. The fitting parameters were the bulk potential in Si, the width of the depleted region and the overall potential drop, as illustrated in Figure S9.

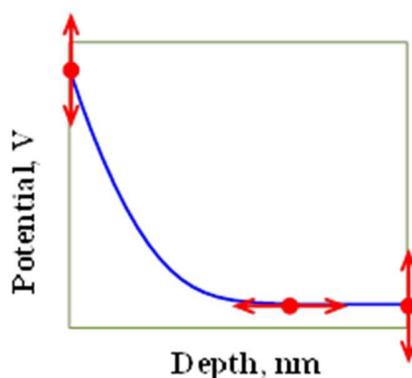


Figure S9. Illustration of the potential shape used for the fitting. Arrows indicate degrees of freedom for the fitting parameters

The regions of confidence for each parameter were defined by t-test for each variable.

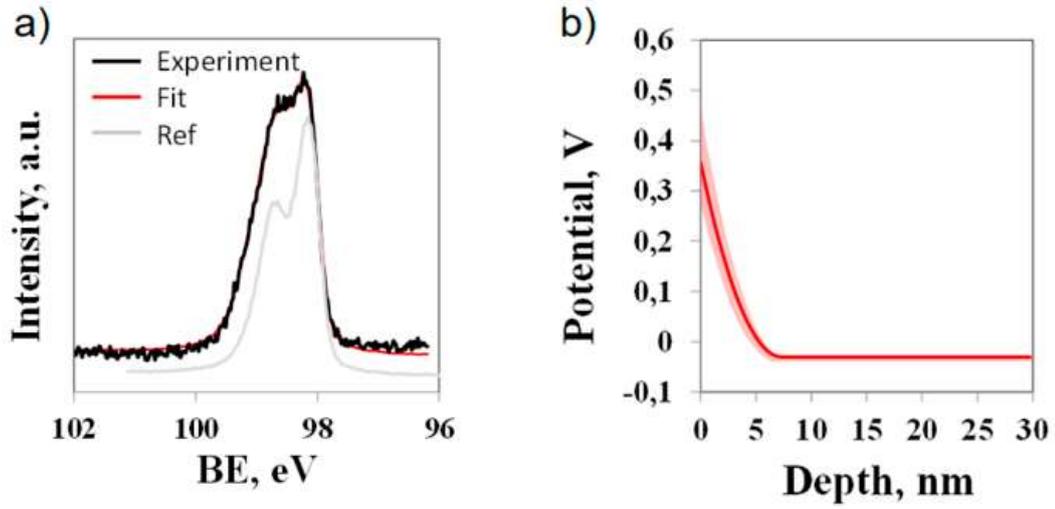


Figure S10. a) The measured Si2p peak (black) from p⁺-Si/HZO/TiN sample along with the potential profile fitting results (red) and the reference spectrum for n⁺-Si sample (gray); b) the obtained potential profile (solid red) with the region of confidence (semi-transparent red)

The electronic band offset diagram was calculated using the experimental data with the help of the well-known methodology(5).⁵ The conduction band offset (CBO) at the Si/HZO interface can be calculated according to the formula (see Figure S11):

$$CBO = E_{g_{HfO_2}} - E_{g_{Si}} + (BE_{Hf4f_{7/2}} - VBM_{HfO_2})_{HfO_2} - (BE_{Si2p} - VBM_{Si})_{Si} - (BE_{Hf4f_{7/2}} - BE_{Si2p})_{HfO_2/Si}$$

where VBM is the valence band maximum, BE – the binding energy, and E_g – the band gap. The band gaps values for HZO, Si as well as the energy separation between BE_{Si2p} and VBM_{Si} were taken from references,⁶⁻⁸ respectively.

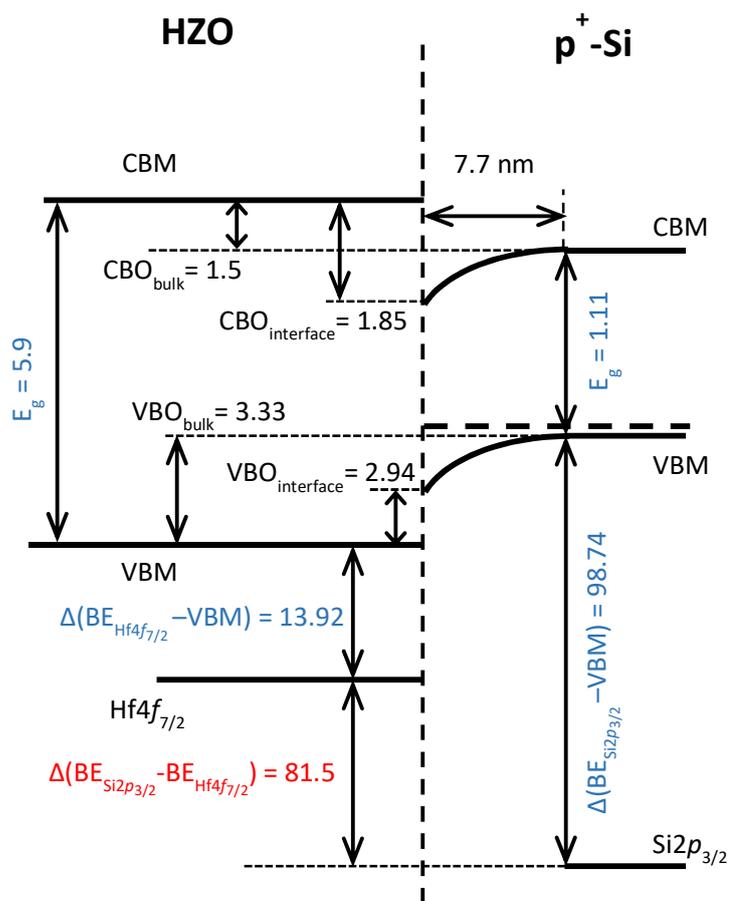


Figure S11. The full electronic band offset diagram for $\text{p}^+\text{-Si}/\text{HfO}_2$, illustrating the methodology for electronic band offset diagram reconstruction

S8 TEMPORAL DYNAMICS OF CHARGE CONCENTRATION AT THE INTERFACE STATES

To qualitatively describe the dynamics of charge accumulation at the interface states, we assume that the trapping-detrapping of these states is characterized by the following capture-emission rates: the internal capture rate g_{nT} defined by temperature, the internal rate of re-emission to the allowed bands r_n , and the external capture rate g_n induced by the external stimulus (specifically, electric field). In this case, the time derivative of the charge accumulated at the interface states is given by the equation^{9,10}:

$$\frac{d\Delta n}{dt} = g_n + g_{nT} - r_n. \quad (2)$$

The internal capture-emission rates define the carriers' lifetime at the interface states:

$$\tau_n = \frac{\Delta n}{r_n - g_{nT}}. \quad (3)$$

The equation (2) transforms to the following one:

$$\frac{d\Delta n}{dt} = g_n - \frac{\Delta n}{\tau_n}. \quad (4)$$

This equation can be solved for Δn , yielding:

$$\Delta n = n_s - C \exp(-t / \tau_n), \quad (5)$$

where $n_s = g_n \tau_n$ is the equilibrium concentration of the charge carriers after the external generation stimulus is applied for a long time, C – the constant defined by the initial conditions, t – time.

If at the given time t_0 the concentration is n_0 and the external generation is turned on, C is defined as:

$$C = (n_s - n_0) \exp(t_0 / \tau_n). \quad (6)$$

Therefore, the concentration increment can be expressed as:

$$\Delta n = n_s - (n_s - n_0) \exp\left(-\frac{t - t_0}{\tau_n}\right). \quad (7)$$

After the external voltage is removed, the space charge region vanishes faster than time required to reach thermal equilibrium in Si. Therefore, one can assume the external generation rate g_n to be equal to zero, i.e., $n_s = 0$ in eq. (5). Thus, if at the given time t_0 the concentration was equal to n_0 , the concentration of the excited (filled) states will be simply described by the following expression:

$$\Delta n = n_0 \exp\left(-\frac{t-t_0}{\tau_n}\right), \quad (8)$$

which defines the charge accumulated at the interface traps.

The result of calculation of the concentration (in arbitrary units) of the charge accumulated at the interface traps for the generation pulses with different delay time is presented in Fig. 5a, where the concentration is expressed in arbitrary units and is normalized to the equilibrium concentration of the charge carriers after the external generation stimulus is applied for a long time.

If the external *ac* voltage is of low frequency, the interface traps have enough time to capture the negative carriers and thus to become excited (i.e., neutralized). The positive charge at Si interface decreases, and the potential drop across FE layer V_{FE} increases (Figure S12, red line).

At high frequency the traps are non-filled, thus they keep positively charged (Figure S12). Applied voltage of 2.5 V induces electric field in FE layer, which is not sufficiently high to reverse polarization. As a result, the measured coercive voltage increases since one needs to apply higher voltage to the device to reach the same coercive electric field across FE layer.

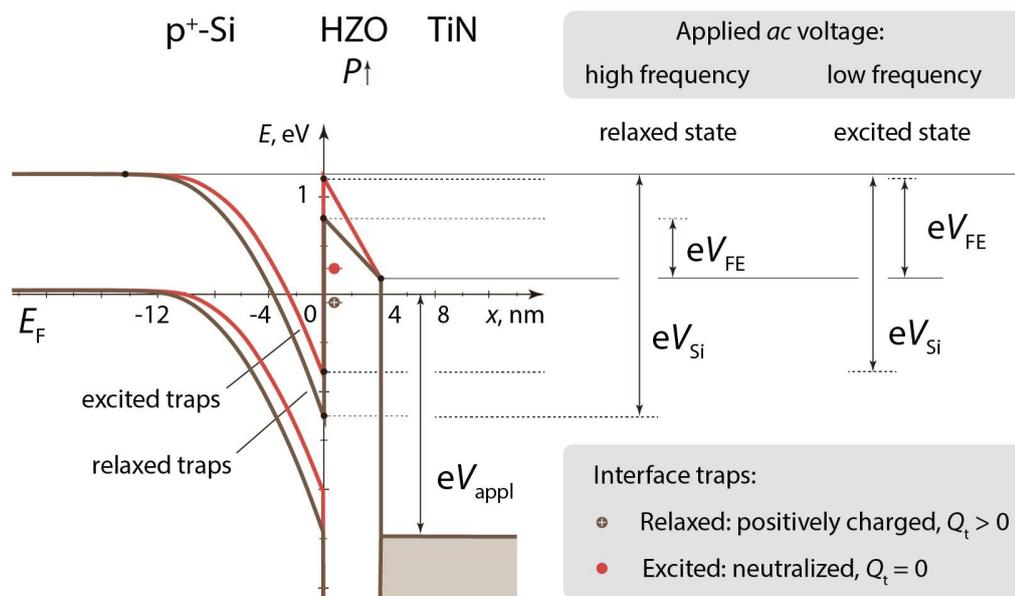


Figure S12. Sketch of band diagrams with different contributions to the potential distribution across p^+-Si/HZO interface at $V_{appl} = 2.5$ V

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