Supporting Information

Gate-Tunable and Programmable n-InGaAs/Black Phosphorus Heterojunction Diodes

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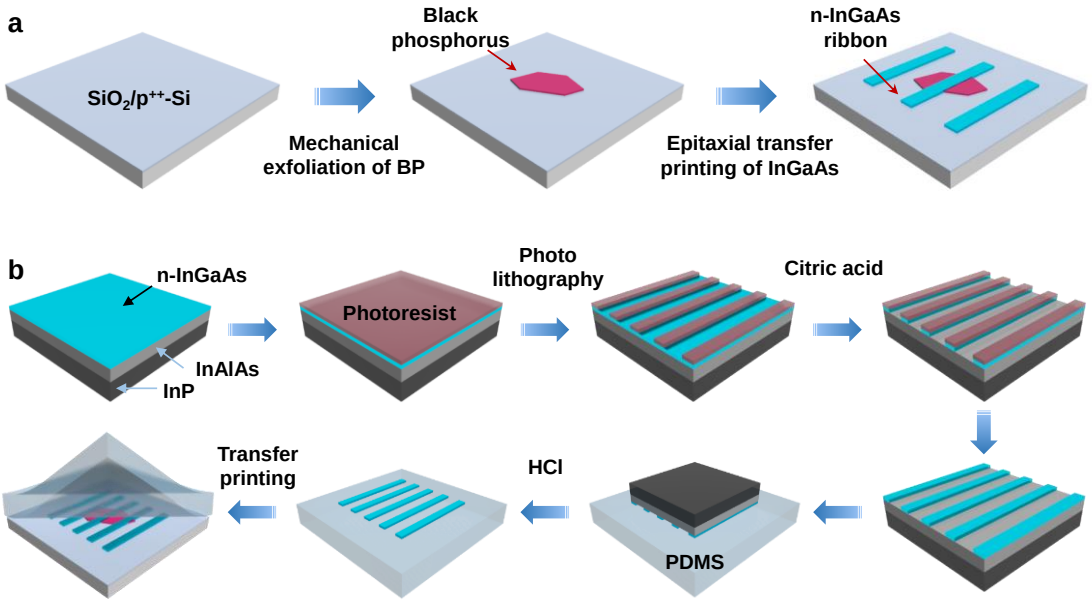

Figure S1. (a) Schematic of the fabrication process of n-InGaAs–BP heterojunction diode. (b) Schematic illustration of details of patterning and transfer printing process of n-InGaAs nanomembrane.

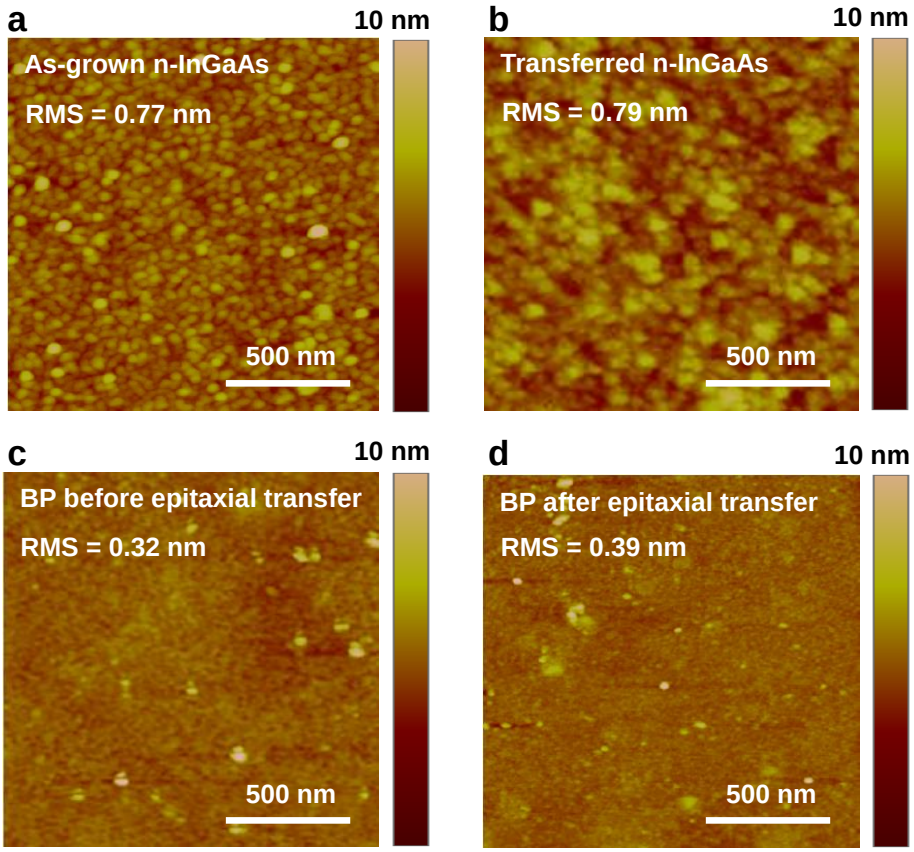

Figure S2. AFM images for the surface roughness of (a) as-grown n-InGaAs and (b) transferred n-InGaAs. AFM images for the surface roughness of BP (a) before the epitaxial transfer printing process of n-InGaAs and (d) after the epitaxial transfer printing process of n-InGaAs.

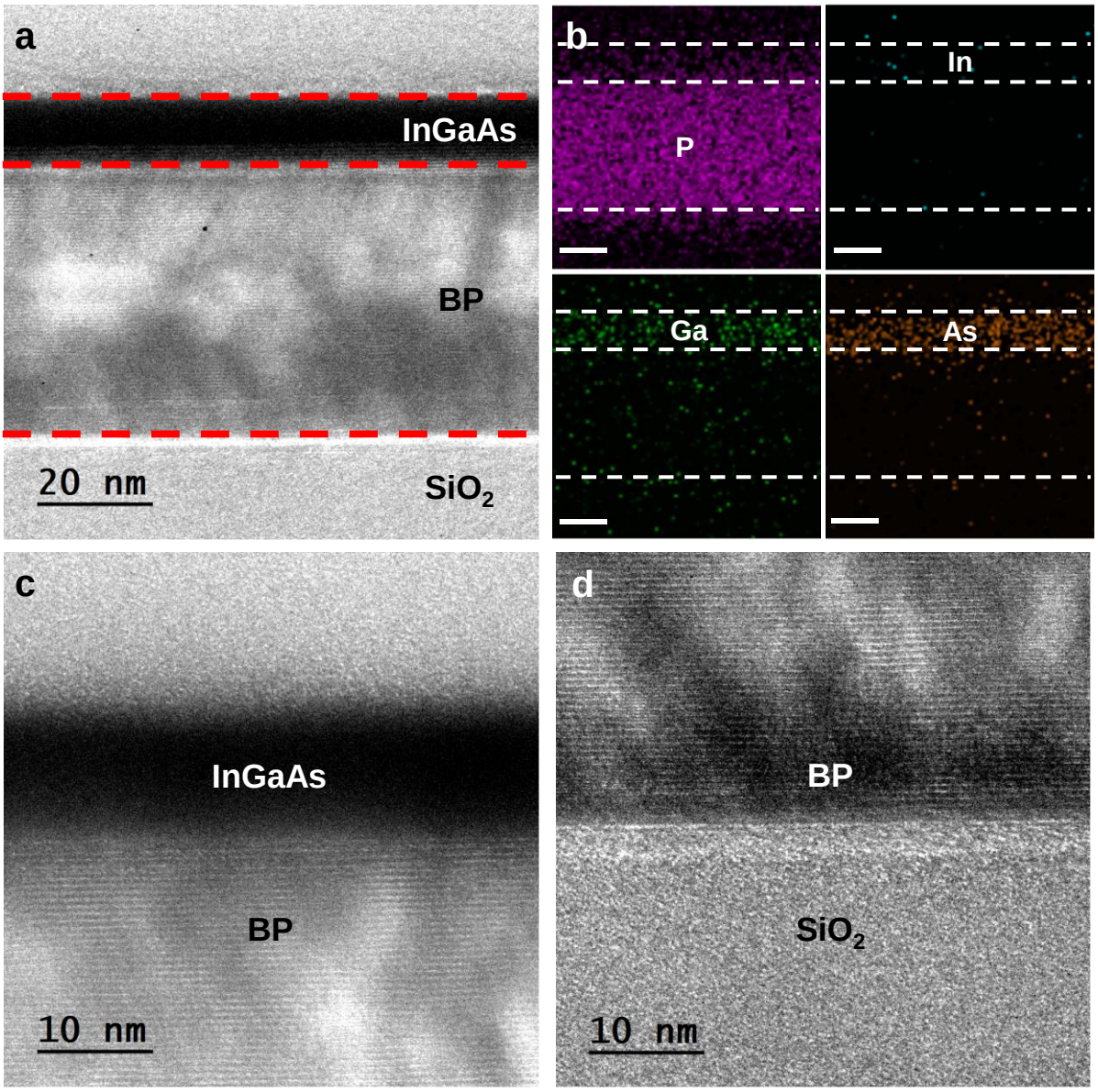

Figure S3. (a) Cross-sectional HRTEM image of n-InGaAs and BP heterojunction. (b) EDS elemental mappings of phosphorus (P), Indium (In), Gallium (Ga), Arsenic (As) of n-InGaAs and BP heterojunction. Scale bar is 10 nm. (c) and (d) Cross-sectional HRTEM images of the interface of (c) InGaAs/BP and (d) BP/SiO_2.

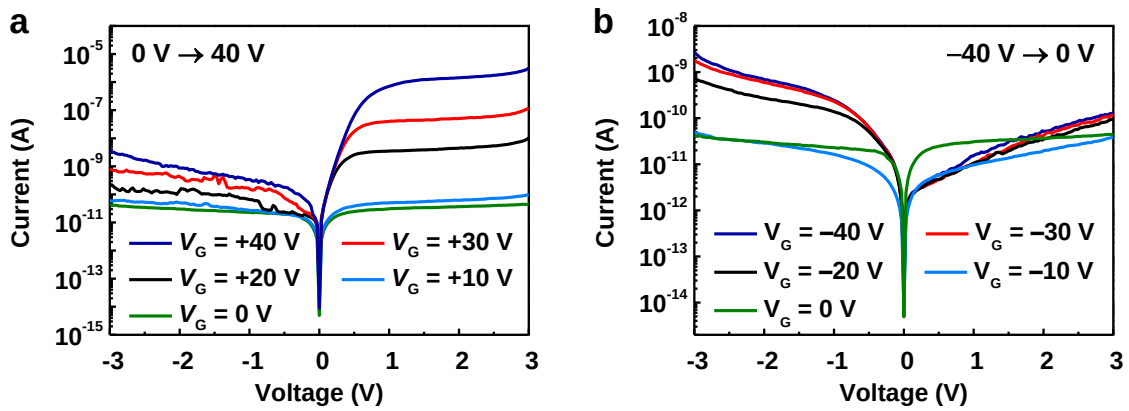

Figure S4. *I-V* characteristics of n-InGaAs–BP heterojunction diode under different gate voltages (a) from 0 to 40 V and (b) from −40 to 0 V.

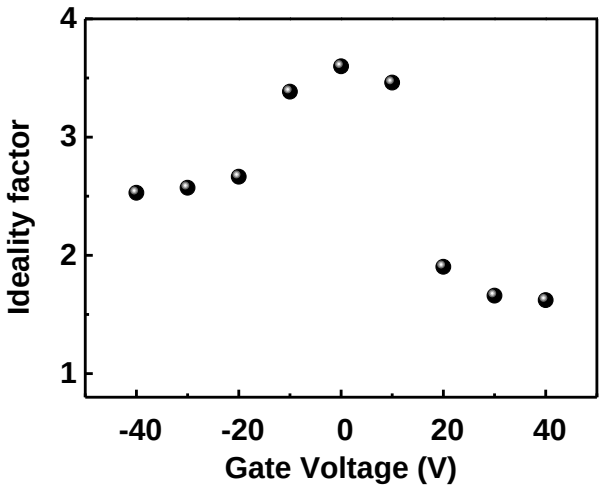

Figure S5. Estimated ideality factor as a function of gate voltages.

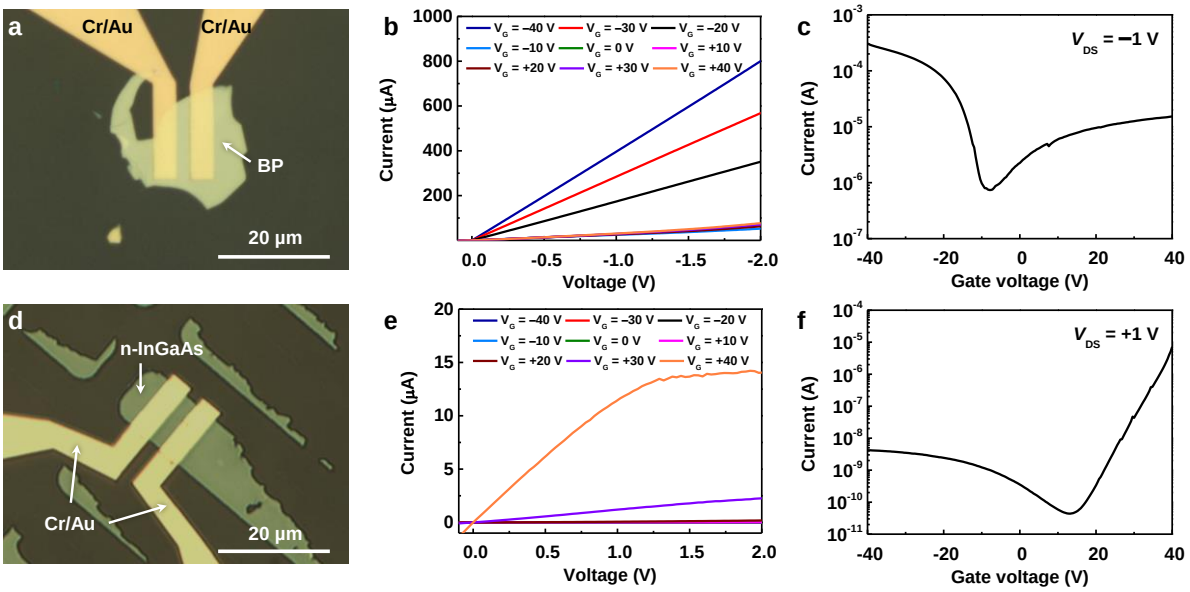

Figure S6. (a) Optical-microscope image and (b) output characteristics of BP FET. (c) Transfer characteristics of BP FET at V_{DS} = −1 V. (d) Optical image and (e) output characteristics of n-InGaAs FET. (f) Transfer characteristics of n-InGaAs FET at V_{DS} = 1 V.

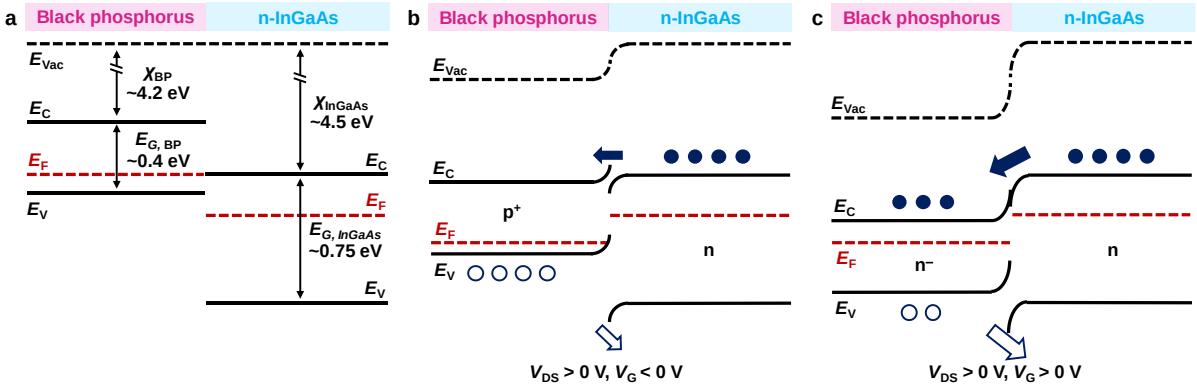

Figure S7. (a) Schematic illustration of estimated band alignment between BP and n-InGaAs. Schematic energy-band diagrams of heterojunction diode under forward bias with (b) negative gate voltage and (c) positive gate voltage. E_{Vac}, E_C, E_V, E_F, E_G and χ are the vacuum level, lowest energy level of the conduction band, the highest energy level of the valence band, the Fermi level, the band gap and the electron affinity of the semiconductors, respectively.

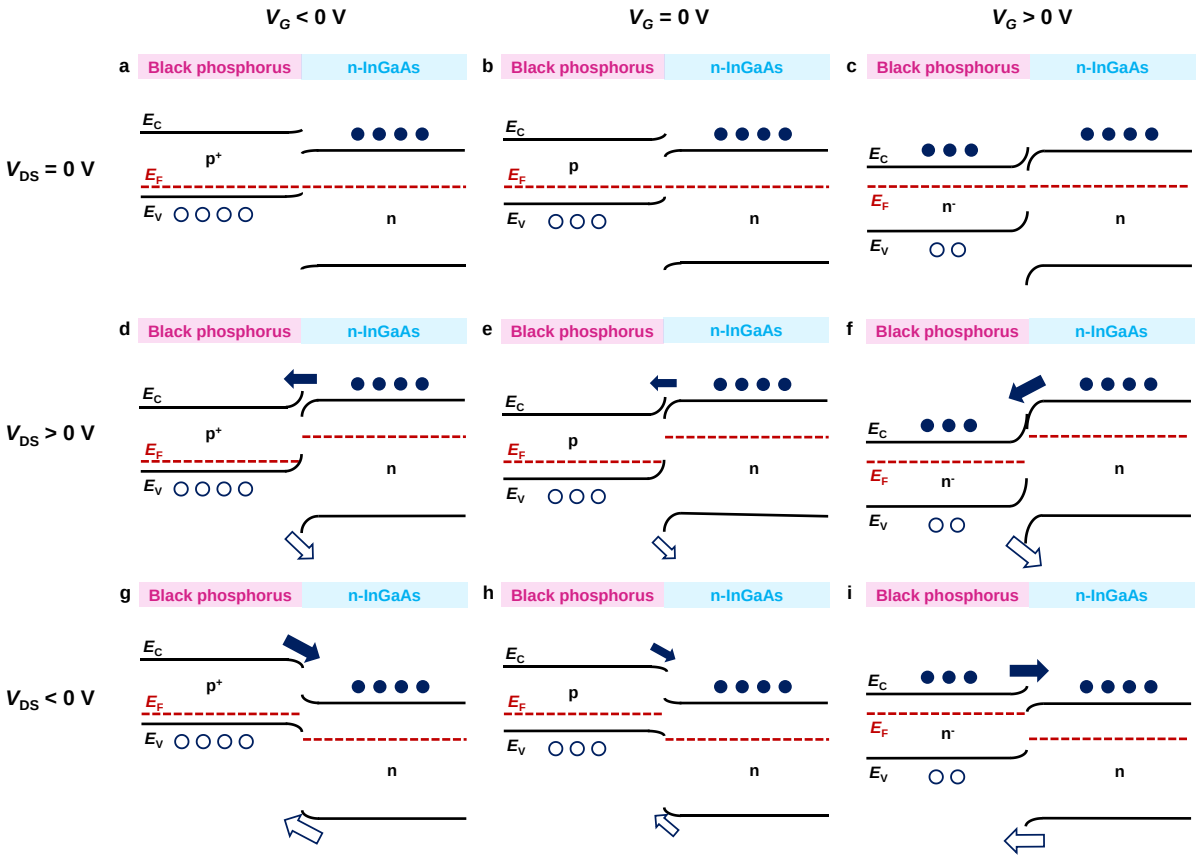

Figure S8. Schematic energy-band diagrams of heterojunction diode under zero bias with (a) negative gate voltage, (b) zero gate voltage and (c) positive gate voltage, under forward bias with (d) negative gate voltage, (e) zero gate voltage and (f) positive gate voltage and under reverse bias with (g) negative gate voltage, (h) zero gate voltage and (i) positive gate voltage.

Change of the energy-band diagrams of n-InGaAs–BP heterojunction diode depending on the bias and gate voltages is shown in Figure S8. Here, the electrostatic inversion of BP nanosheets from p-type to n-type as the gate voltage change from negative to positive induces the modulation of the Fermi level of BP, whereas the Fermi level of n-InGaAs remains stationary due to the Fermi-level pinning effect. These behaviors induce the change of the band structure and electrical transport in the heterojunction diode (Figures S8a–c).[1] Here, the band bending of BP at the interface occurs due to the weak Fermi-level pinning which is caused by the defect

and vacancy of molecules in the surface.[2] Due to the modulation of the band structure, the current flow of the heterojunction diode depends on the gate and applied bias voltages. Especially, under the forward bias, the current of device increases at the positive gate voltage due to the decreased barrier height. On the other hand, the flow of holes from BP to InGaAs is dominantly blocked by the barrier at the negative gate voltage, resulting in low current levels as shown in Figures S8d–f. While under reverse bias, the change of current in the device is much smaller than under forward bias because the current flow is blocked by the barrier at positive gate voltage and depends on minority carriers at the negative gate voltage (Figures S8g–i).

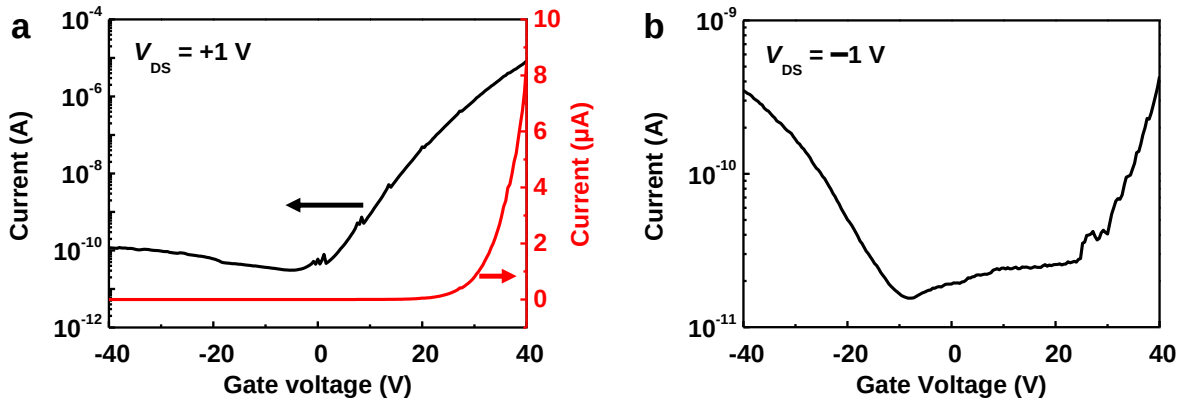

Figure S9. a) Transfer characteristics of n-InGaAs–BP heterojunction diode at V_{DS} = 1 V on a linear scale (red) and on a semi-logarithmic scale (black). b) Transfer characteristics of n-InGaAs–BP heterojunction diode at V_{DS} = −1 V on a semi-logarithmic scale.

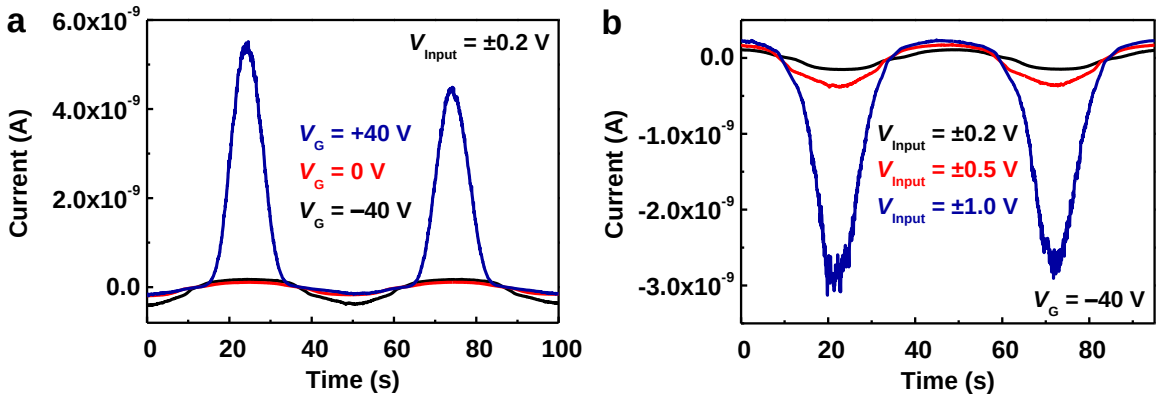

Figure S10. (a) Output current of heterojunction diode with sinusoidal input drain-source voltage (V_{Input} = −0.2 to +0.2 V) and under applied gate voltages of −40, 0, 40 V. (b) Output current of heterojunction diode under applied gate voltage of −40 V and with sinusoidal input drain-source voltages of various magnitudes (V_{Input} = −1 to +1, −0.5 to +0.5, and −0.2 to +0.2 V).

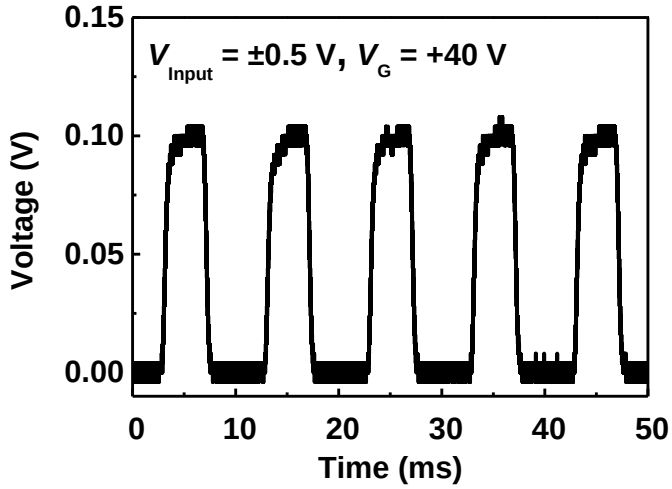

Figure S11. Output voltage of n-InGaAs–BP heterojunction diode with external resistor (R = 1 MΩ) under applied gate voltage of 40 V and sinusoidal input drain-source voltage (V_{Input} = −0.5 to 0.5 V; 0.1 kHz).

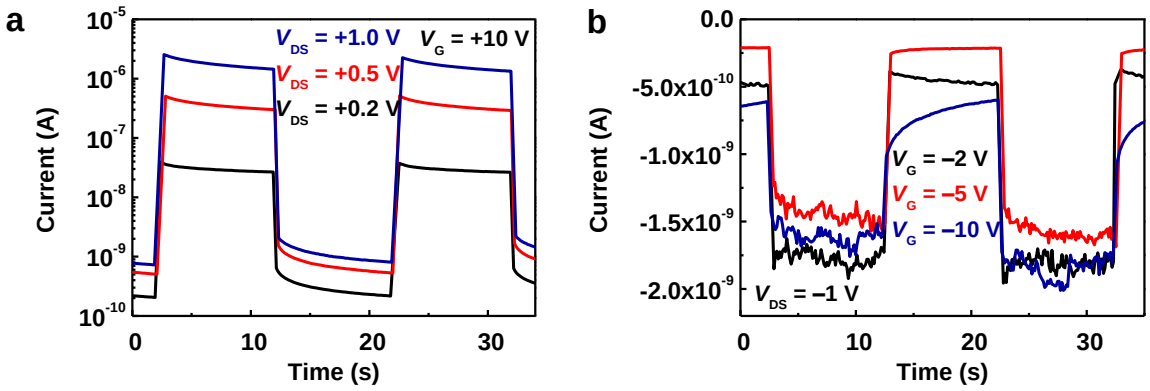

Figure S12. (a) Output current of heterojunction diode with rectangular voltage pulse applied to gate (V_G = 10 V) under forward biases of 0.2, 0.5, and 1 V. (b) Output current of heterojunction diode under reverse bias of −1 V and with rectangular voltage waveform of various magnitudes applied to gate (V_G = 2, 5, and 10 V).

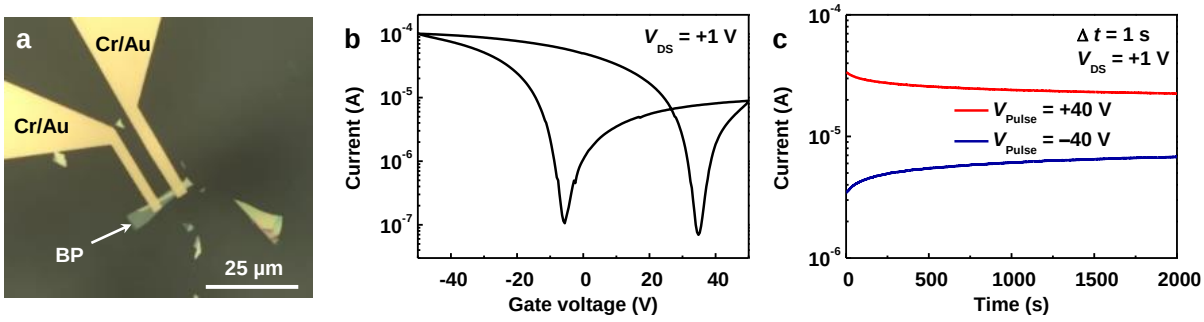

Figure S13. (a) Optical-microscope image of BP FET. (b) Transfer characteristics of BP FET under forward bias of 1 V with gate voltage sweep from −50 V to 50 V in positive direction and 50 V to −50 V in negative direction. (c) Retention test of BP FET under forward bias of 1 V with ±40 V applied gate voltage pulses for 1s.

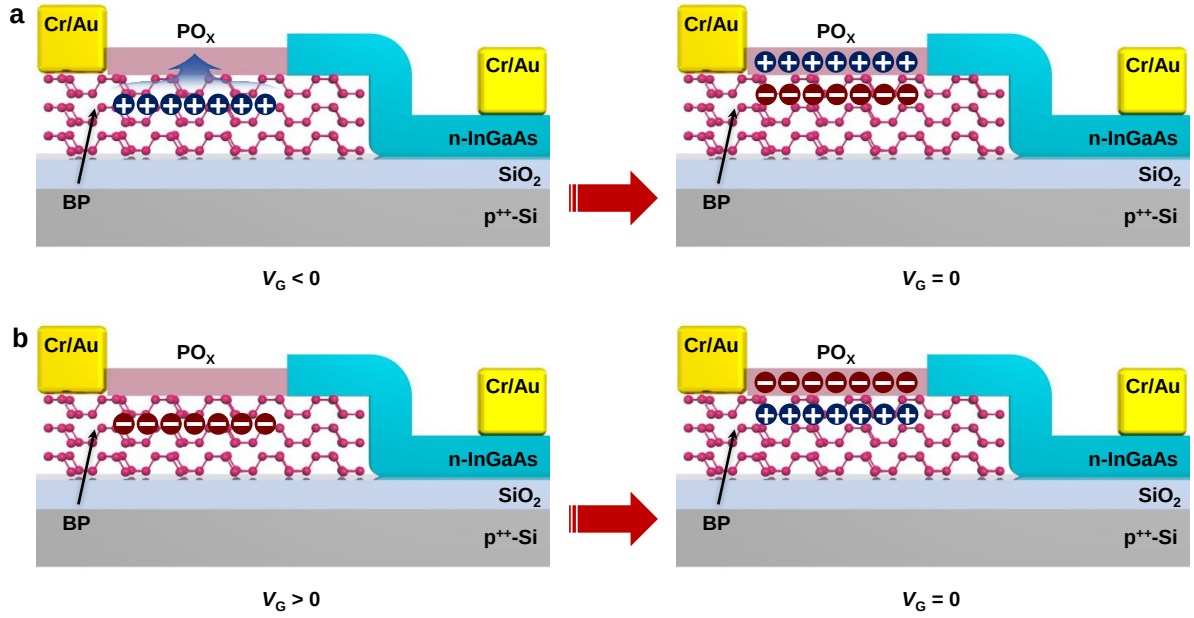

Figure S14. Schematics of programmable heterojunction diode in (a) programmed state and (b) erased state.

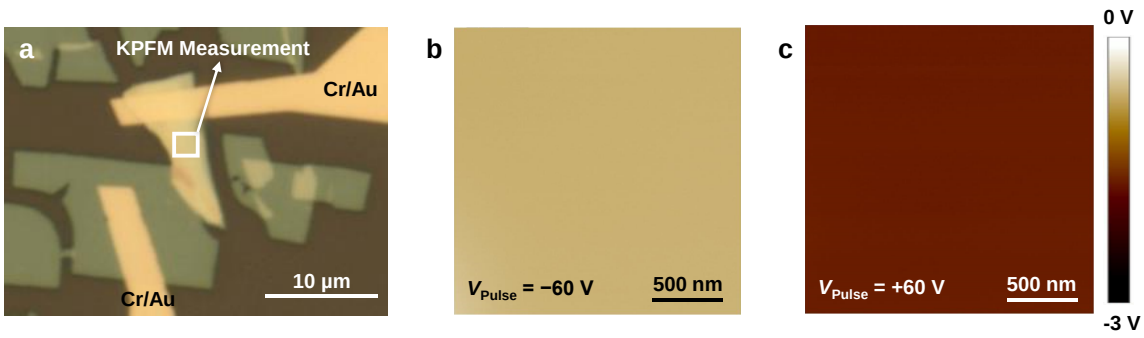

Figure S15. (a) Optical-microscope image of n-InGaAs–BP heterojunction diode used for Kelvin probe force scope measurement (KPFM). (b) KPFM image on BP with V_{CPD} ~ −0.59 V after the device is programmed by −60 V applied gate voltage pulses for 1s. (c) KPFM image of BP with V_{CPD} ~−1.65 V after device is erased by 60 V applied gate voltage pulses for 1s.

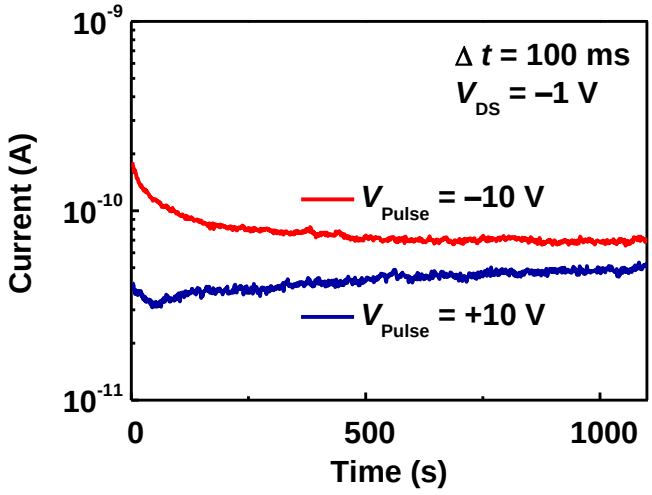

Figure S16. Retention test of n-InGaAs–BP heterojunction diode under reverse bias of −1 V with ±10 V applied gate voltage pulses for 100 ms.

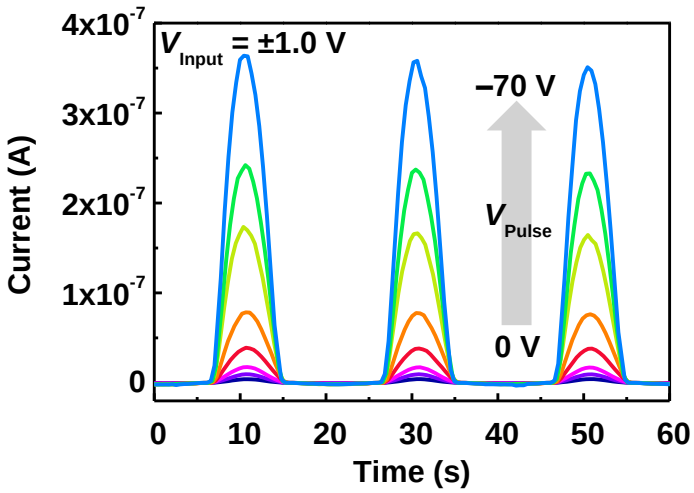

Figure S17. Output current of n-InGaAs–BP heterojunction diode with sinusoidal input drain-source voltage (V_{Input} = −1 to +1 V) and 10 s gate voltage pules ranging from 0 to −70 V.

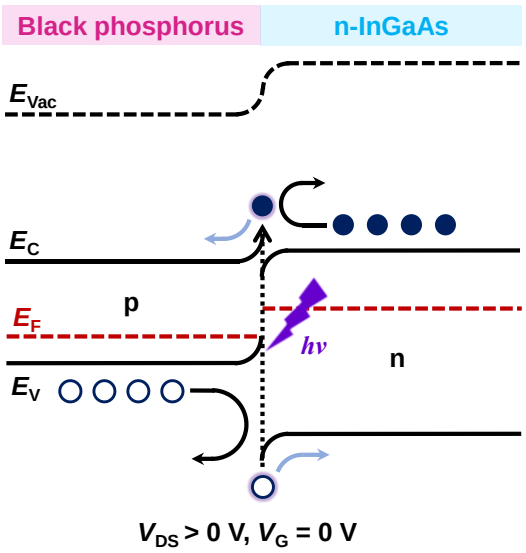

Figure S18. Schematic of energy-band diagram of heterojunction diode under forward bias and zero gate voltage.

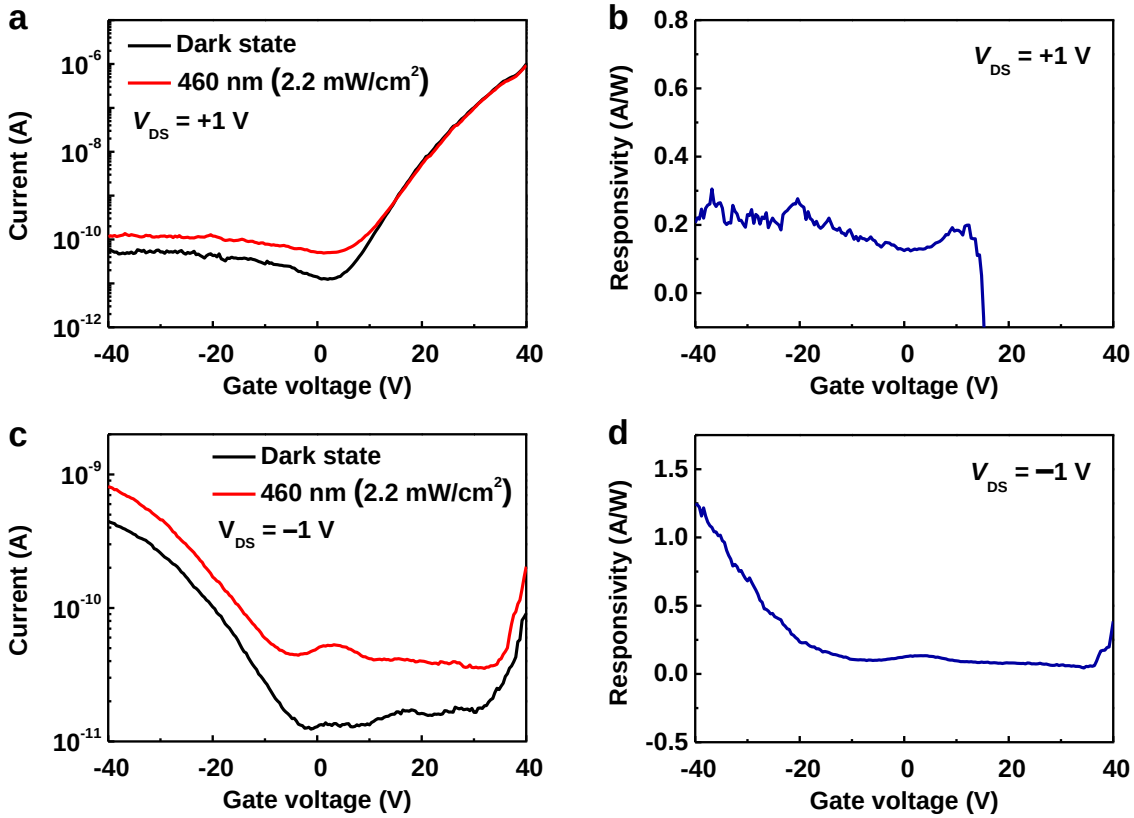

Figure S19. (a) Transfer characteristics of n-InGaAs–BP heterojunction diode under forward bias of 1 V in dark and 460 nm light illumination. (b) Responsivity of n-InGaAs–BP heterojunction diode under forward bias of 1 V as a function of gate voltage. (c) Transfer characteristics of n-InGaAs–BP heterojunction diode under reverse bias of −1 V in dark and 460 nm light illumination. (d) Responsivity of n-InGaAs–BP heterojunction diode under reverse bias of −1 V as a function of gate voltage.

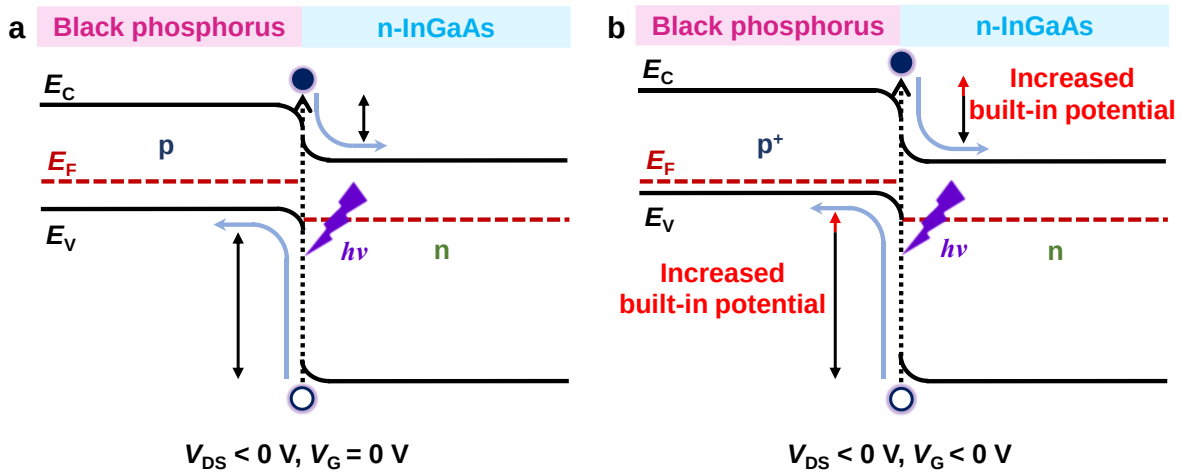

Figure S20. Schematic illustration of energy-band diagrams of heterojunction diode under reverse bias with light illumination under (a) zero gate voltage and (b) negative gate voltage states.

Table S1. Comparison of possible functionalities of various multi-functional devices.

Structure	Diode	Transistor	Memory	Photodetector	Logic system	Ref.
BP/InGaAs heterojunction	R_{rec}: 4600	M: 84.6 $cm^2 V^{-1} s^{-1}$; On/Off ratio: ~10^5	T_r: 1000 s	R_{ph}: 0.704 A/W	ADDER	This work
Si/SWNT heterojunction	—	On/Off ratio: ~10^5	—	R_{ph}: ~1 A/W	AND; OR; ADDER	3
BP-MoS_2 heterostructure	R_{rec}: ~4 ×10^5	On/Off ratio: ~10^7	—	—	Inverter	4
MoS_2-$MoTe_2$ heterostructure	R_{rec}: ~10^7	On/Off ratio: ~10^8	R_{pr}: ~10^9	R_{ph}: ~28.6 A/W	—	5
Graphene-MoS_2 heterostructure	—	M: ~10^4 $cm^2 V^{-1} s^{-1}$	T_r: ~4 × 10^4 s	R_{ph}: ~5 × 10^8 A/W	—	6
Multilayer /Monolayer MoS_2 heterojunction	R_{rec}: ~10^3	M: 0.1–10 $cm^2 V^{-1} s^{-1}$; On/Off ratio: ~10^7	—	R_{ph}: ~10^3 A/W	—	7
Layer-controlled BP heterojunction	—	M: 100 $cm^2 V^{-1} s^{-1}$; On/Off ratio: ~10^6	—	R_{ph}: 383 A/W	—	8

R_{rec}: Rectifying ratio, M: Mobility, T_r: Retention time, R_{ph}: Photo-responsivity, R_{pr}: Program/erase ratio

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