Supporting information

Wafer Scale Growth and Characterization of Edge Specific Graphene Nanoribbons for Nanoelectronics

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Supporting note 1: Etching and growth reactors

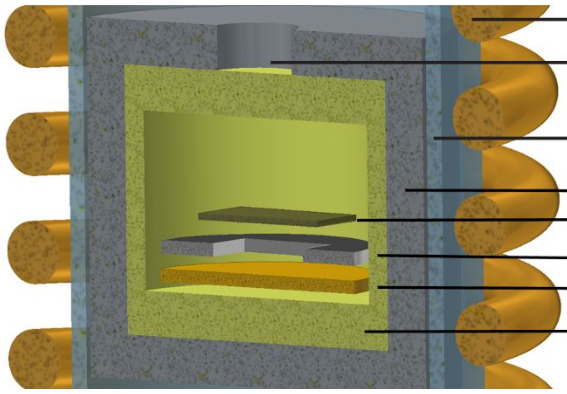

Fig.S1. Schematics of the reactor used for thermal etching and graphene growth

In Fig.S1 a schematics of the etching reactor is depicted. Ta foil plays a key role to provide a Si rich ambient preventing Si escape and graphene growth. For the growth of graphene, the samples were annealed in a similar inductively heated furnace without Ta foil. Homogeneous graphene growth in the reactor has been demonstrated on the wafer (2inch) scale.

Supporting note 2: Micro-diffraction study of arm-chair graphene nanoribbons

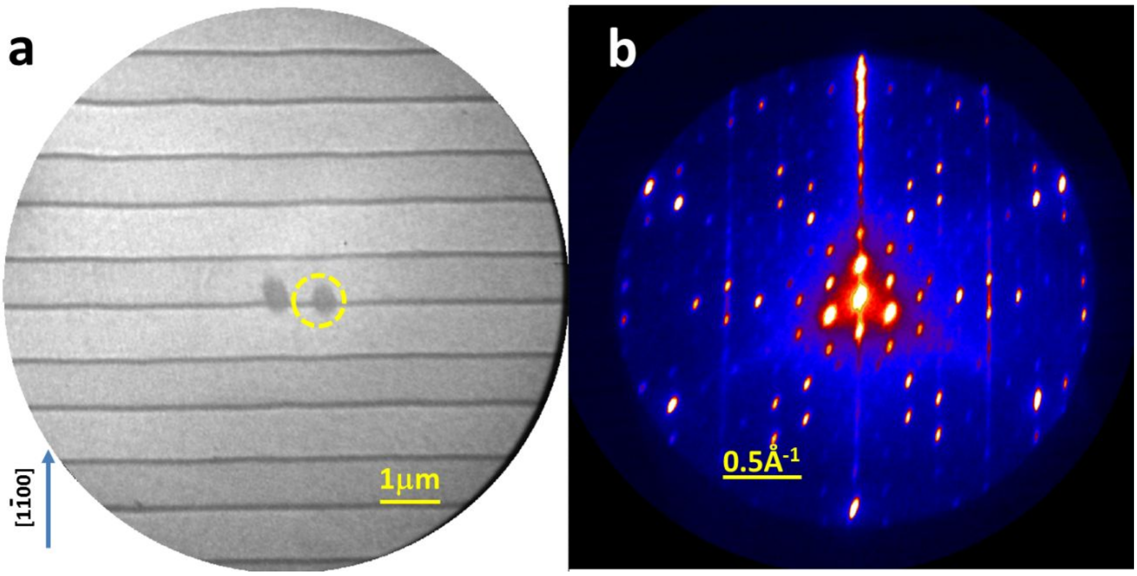

Fig.S2. LEEM and micro-LEED studies of the AC GNRs. a) Bright field LEEM image (FoV=10μm, E=5eV), black marks in the center shows sampling area (400nm) for the micro-LEED from single AC mesa wall; b) μ-LEED pattern (E=29.5eV) from a single mesa wall. The facet spots from the AC graphene ribbons clearly seen along with 6Sqrt3 reconstruction, the most widely accepted characteristic of the buffer layer grown on Si-face of SiC.

Supporting note 3: Fast Fourier transform of the STM data for ZZ and AC GNR

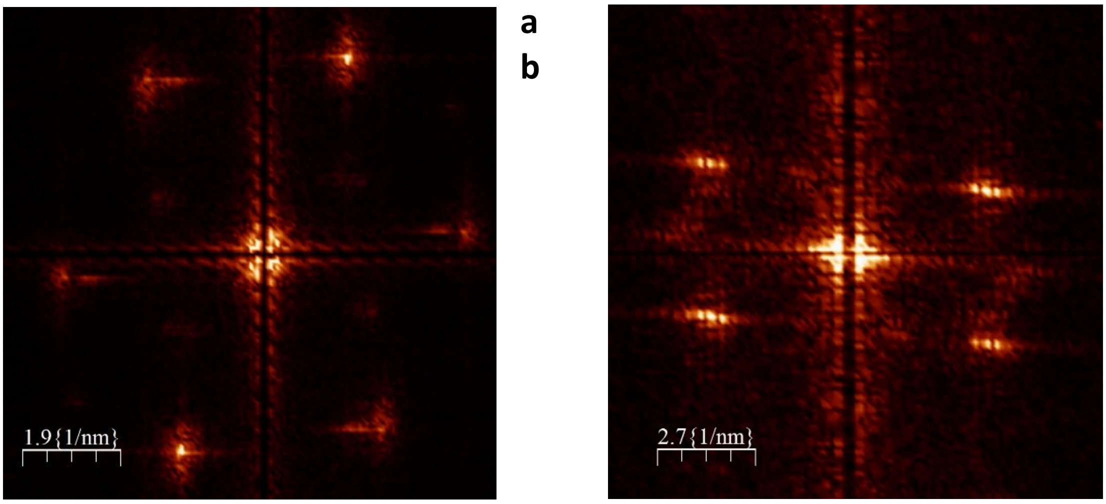

Fig. S3 Fast Fourier transform of the STM data, shown in Fig. 3d (a) and 4d (b) for ZZ and AC GNRs, respectively. A slight shear distortion of the patterns due to the mechanical drift of the sample and creep of the piezoceramic actuator is visible in both patterns. The set of satellite spots around the principle graphene spots in S3 b originates from the micro steps periodicity.