Supplementary Information for

Complementary Black Phosphorus Tunneling Field-Effect Transistors

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1. Thickness determination of BP

It is well known that BP readily oxidizes and forms PO_x upon exposure to air by reacting with oxygen and water.[1,2,3] In addition to air exposure during the device fabrication process, the BP surface was also exposed to a water rich environment at elevated temperatures (200 °C) during the ALD gate oxide deposition. Since the electrically active BP layer thickness is a critical parameter for the tunneling currents in our devices, it is important to determine the thicknesses of the oxidized layers and the thickness of the remaining crystalline BP layer in the total BP flake thickness.

Figure S1(a) shows an AFM image and line scan of a t_{body}=8.3 nm thick BP flake as the active channel in one of the BP RED-TFETs with a nominal t_{ox}=5.6 nm thick Al_2O_3/HfO_2 gate dielectric stack as described in the manuscript. Figure S1(b) shows a comparison of the experimentally measured I_d-V_g curve of this device and a set of simulations with different flake thicknesses. In our simulations, we have considered both the reduction of the body thickness and the increase of the oxide thickness as a result of oxidation, and we assume the resulting PO_x layers on the top and on the bottom side of BP are of the same thickness (note that only the PO_x layer on the top contributes to the gate dielectric thickness t'_{ox}). The dielectric constants of the oxides used in the simulation are 8 for Al_2O_3, 16 for HfO_2 and 5.4 for PO_x. The chemical composition of the PO_x layer formed on black phosphorus is assumed to be P_2O_5 (ref. 3) and the dielectric constant is estimated from phosphate glass,[4] in which P_2O_5 acts as glass former. As apparent from Figure S1(b), a body thickness of t'_{body}=3 nm and a t'_{ox}=8.3 nm (t_{ox}=5.6 nm, plus additional 2.7 nm of PO_x layer) results in the best match between experiment and simulation.

To verify our assumption of a substantial reduction in BP body thickness and corresponding increase of dielectric layer thickness through the formation of PO_x, a careful TEM analysis on another BP RED-TFET that went through the same fabrication process was performed. The BP flake thickness in this device is determined to be t_{body}=12.8 nm from AFM measurements, as shown in Figure S1(c). Figure S1(d) shows an HAADF-STEM image of the BP RED-TFET. Figure S1(e) shows higher magnification HAADF-STEM images of the "G1-S" and "G1" regions, as depicted by the red and green boxes in Figure S1(d). The thicknesses of the BP crystalline layer and PO_x layers are labeled in the images, which are determined using the method described below.

Figure S1(f) shows an electron energy loss spectrum (EELS) in the "G1-S" region, which is the sum of all the background subtracted spectra acquired along the A-B line depicted in Figure S1(e), showing the P-*L*, O-*K* and Ti-*L* edges. Figure S1(g) shows the intensity profiles of the HAADF image (HAADFI) and EELS P-*L*, O-*K* and Ti-*L* edges along the A-B line in Figure S1(e). Combining the HAADF intensity profile and EELS line scan, one can determine the thicknesses of the top PO_x layer and the BP crystalline layer in the "G1-S" region to be 1.4 nm and 6.9 nm respectively. The total flake thickness is 13 nm, which agrees reasonably well with the AFM measurement. Using the same method, we can measure the thicknesses of the top PO_x layer and the BP crystalline layer in the "G1" region to be 1.9 nm and 6.7 nm respectively, with the total flake thickness being 12.2 nm. The discrepancy between the extraction in the G1-S and G1 region occurs reasonable considering the variations when preparing the sample for cross-section TEM and the uncertainty in determining the position of the interface between PO_x and SiO_2.

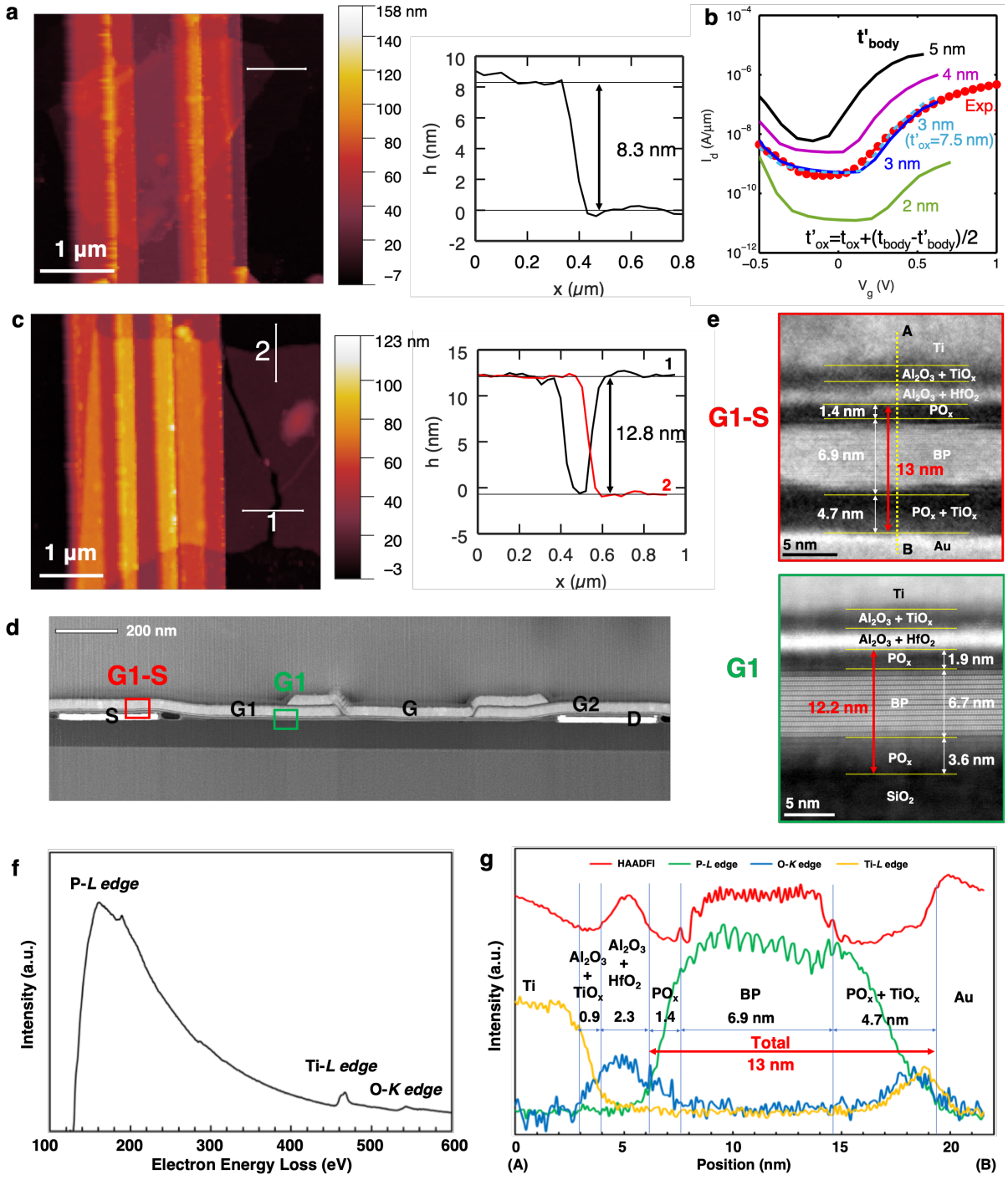

Figure S1. Thickness determination of BP. (a) AFM image and line scan of the BP flake used in the electrical characterization (t_{body}=8.3 nm). (b) Comparison of measured I_d-V_g curve of BP TFET (dots) and simulated I_d-V_g curves for different body thicknesses t'_{body} (lines). The simulation with t'_{body}=3 nm matches best with the experiment. (c) AFM image and line scan of the BP flake used in the TEM analysis (t_{body}=12.8 nm). (d) HAADF-STEM image showing the cross-section of the BP RED-TFET. (e) Higher magnification HAADF-STEM images from the regions defined by the red and green boxes in (d). (f) Background subtracted EELS spectra, showing the sum of all the spectra acquired along A-B line shown in (e). (g) Intensity profiles of HAADF image and EELS P-*L*, O-*K* and Ti-*L* edges along A-B line in (e), showing the thicknesses of crystalline BP and PO_x layers and total flake thickness.

In conclusion, from the TEM analysis, we have found that in a t_{body}=12.8 nm thick BP flake, the thickness of the BP crystalline layer is reduced to t'_{body}=6.9 nm. This means that in the t_{body}=8.3 nm thick BP flake, the BP crystalline layer thickness should be about t'_{body}=2.4 nm [~ 8.3 nm – (12.8 nm – 6.9 nm)]. Considering the uncertainty in the thickness measurements and device-to-device variations, t'_{body}=3 nm is a good approximation for the simulation framework employed in Figure S1(b). Note that to account for the thickness of the PO_x layer (~1.9 nm from the TEM analysis), the effective dielectric thickness of the Al_2O_3/HfO_2 plus PO_x gate dielectric stack is corrected to be t'_{ox}=7.5 nm (~ 5.6 nm + 1.9 nm) which is decomposed in the atomistic simulation into the various oxide layers.

2. Drain doping impact on ambipolar branch of the BP RED-TFET

Figure S2(a) shows the impact of drain doping on the ambipolar branch of the BP RED-TFET in n-type TFET mode. In the BP RED-TFET, the drain doping is achieved through electrostatic doping controlled by G2. Therefore, by tuning V_{g2} we can change the doping type and concentration in the drain region.

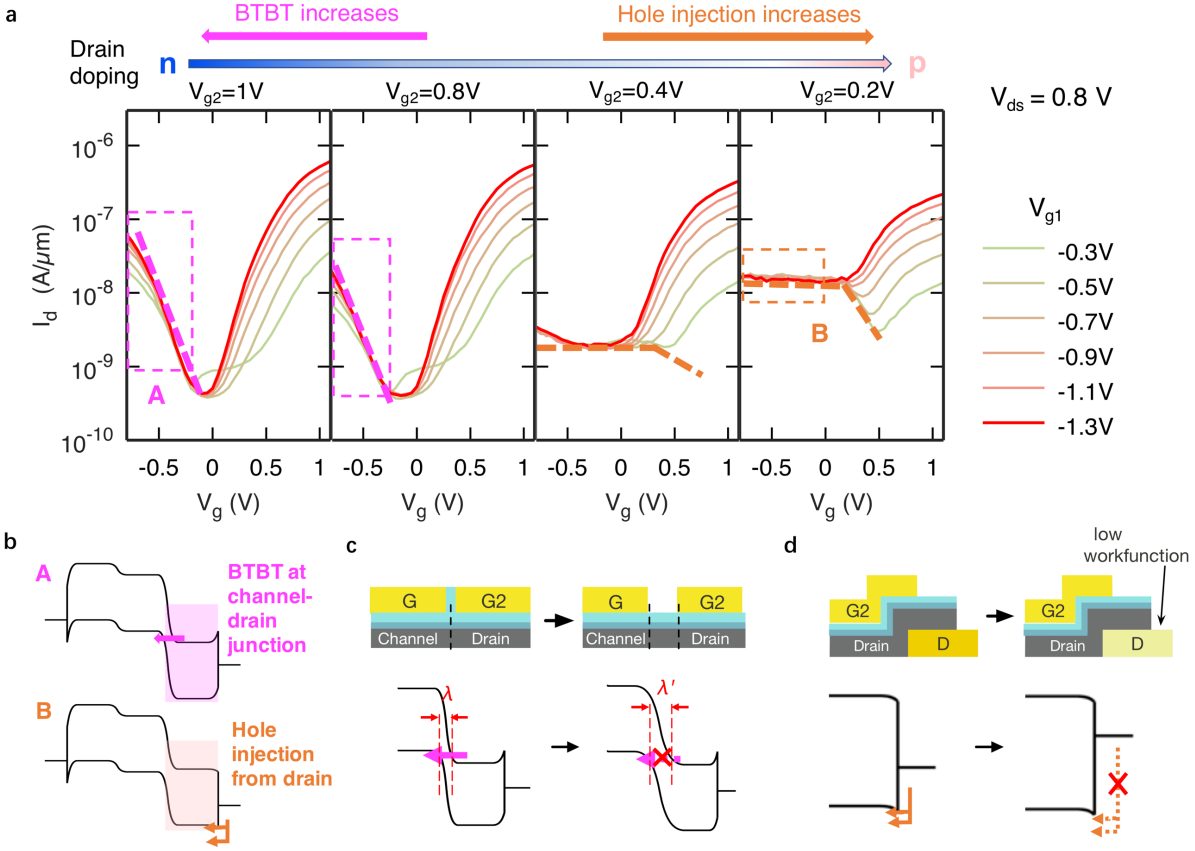

Figure S2. Drain doping impact on ambipolar branch of the BP RED-TFET. (a) Transfer characteristics of RED-TFET with different drain doping conditions, showing ambipolar currents due to two different carrier injection mechanisms. (b) Band diagrams for the two mechanisms of ambipolar currents: BTBT at the channel-drain junction and hole injection from drain. (c) Design for suppressing ambipolar BTBT by increasing tunneling distance at drain-channel junction. (d) Design for suppressing ambipolar drain injection by using a low workfunction drain contact.

First, when we apply V_{g2} = 1V, the drain is doped n-type, and when V_g is negative, there exists a BTBT tunneling path from the channel region to the drain, as is shown in the band diagram labeled with "A" in Figure S2(b). Therefore, in the transfer characteristics, we see an ambipolar branch corresponding to this BTBT current. When V_{g2} decreases to 0.8V, the n-doping in the drain region becomes weaker, and the ambipolar tunneling current becomes smaller, as can be seen from the transfer characteristics. However, if we further decrease V_{g2}, the drain doping decreases and eventually becomes p-doped, and the hole injection from the drain contact (both thermionic injection and tunneling through Schottky contact) becomes stronger, as is shown in the band diagram labeled with "B" in Figure S2(b). Therefore, both mechanisms A) ambipolar BTBT at the channel-to-drain junction and B) ambipolar hole injection from drain need to be addressed through proper choice of the drain doping to achieve the lowest possible OFF-current.

The ambipolar branch can be suppressed with an improved design of the RED-TFET. By introducing an underlap between the channel and drain regions,[5] or equivalently between G and G2 in the RED-TFET, the tunneling distance for BTBT between the channel and drain region is increased, as is shown in Figure S2(c), and therefore the ambipolar BTBT gets suppressed. The hole injection can be suppressed by increasing the Schottky-barrier height for hole injection at the drain, which can be achieved by using a low work function contact metal, as is shown in Figure S2(d).

3. Hysteresis in transfer characteristics of the BP RED-TFET

Figure S3 shows the transfer characteristics of a BP RED-TFET under two scan directions – solid line swept from 1.1 V to -0.6 V, and dashed line swept from -0.6 V to 1.1 V. The step in V_G is 0.05 V. In the electrical measurement, we set the integration time to "SHORT" when using the Agilent 4156C Parameter Analyzer and the scan rate is about 1 V/s. As can be seen from Figure S3, the hysteresis is less than 50mV, indicating a good-quality gate oxide has been formed on BP.

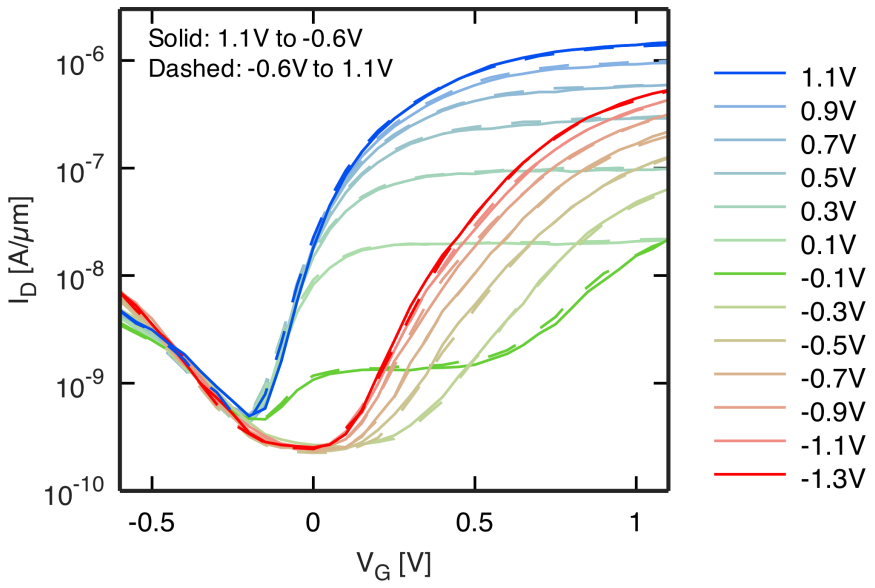

Figure S3. Hysteresis of transfer characteristics of the BP RED-TFET

4. Gate leakage current of the BP RED-TFET

Figure S4 shows the gate leakage currents of all three gates, G1, G2 and G, in the BP RED-TFET operating in MOSFET and TFET modes. All of the gate currents are more than one order-of-magnitude smaller than drain currents, which implies that the drain currents and SS extraction in this work are not impacted by gate leakage. Also note that most of the leakage currents result from leakage between gates (where $I_g = I_{g1}$ or $I_g = I_{g2}$), and the gate-to-channel leakage currents are accordingly even smaller.

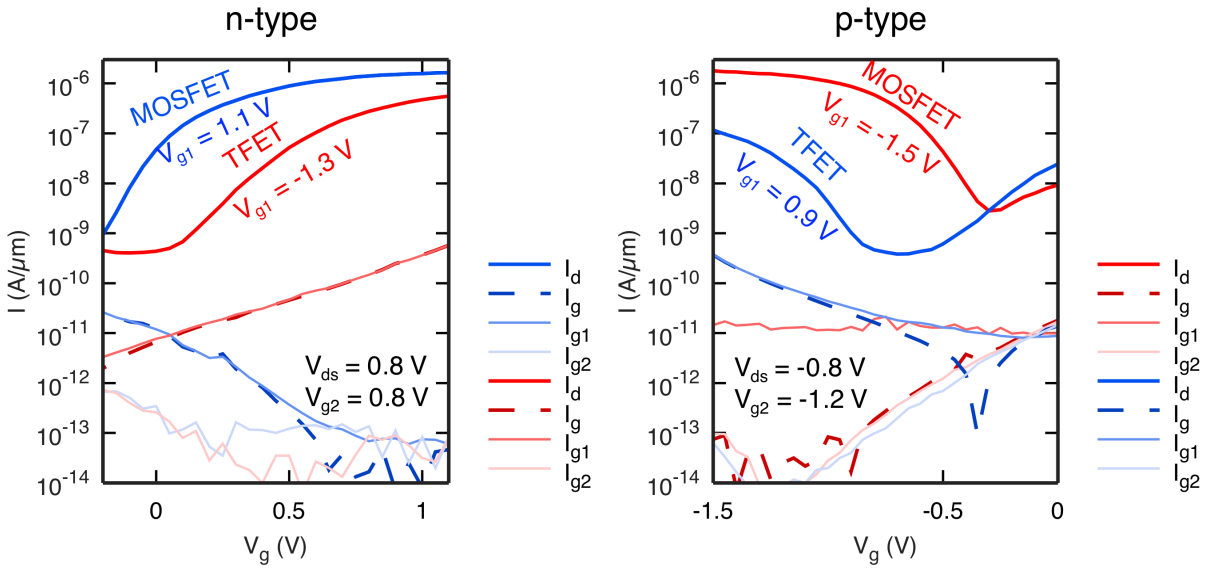

Figure S4. Gate leakage currents of the BP RED-TFET

5. Stability of black phosphorus

As mentioned in Section 1, BP readily oxidizes upon exposure to air, and the electrical properties of BP degrade with oxidation. Previous studies also show that the air stability of BP can be improved by means of passivation.[2,6,7] We found that the electrical properties of black phosphorus devices are rather stable if samples are stored in an inert environment or properly passivated.

Figure S5(a) shows the transfer characteristics of a BP RED-TFET measured immediately after fabrication and after storage in a nitrogen dry box for 4 months. The characteristics remain almost unchanged, except for a slight shift in threshold voltage.

We also studied the passivation of BP for achieving air-stable devices. 20 nm thick Al_2O_3 was grown on a BP FET using ALD to passivate the device. As is shown in Figure S5(b), the characteristics of the BP FET remain stable after storage in air over a time period of 180 days.

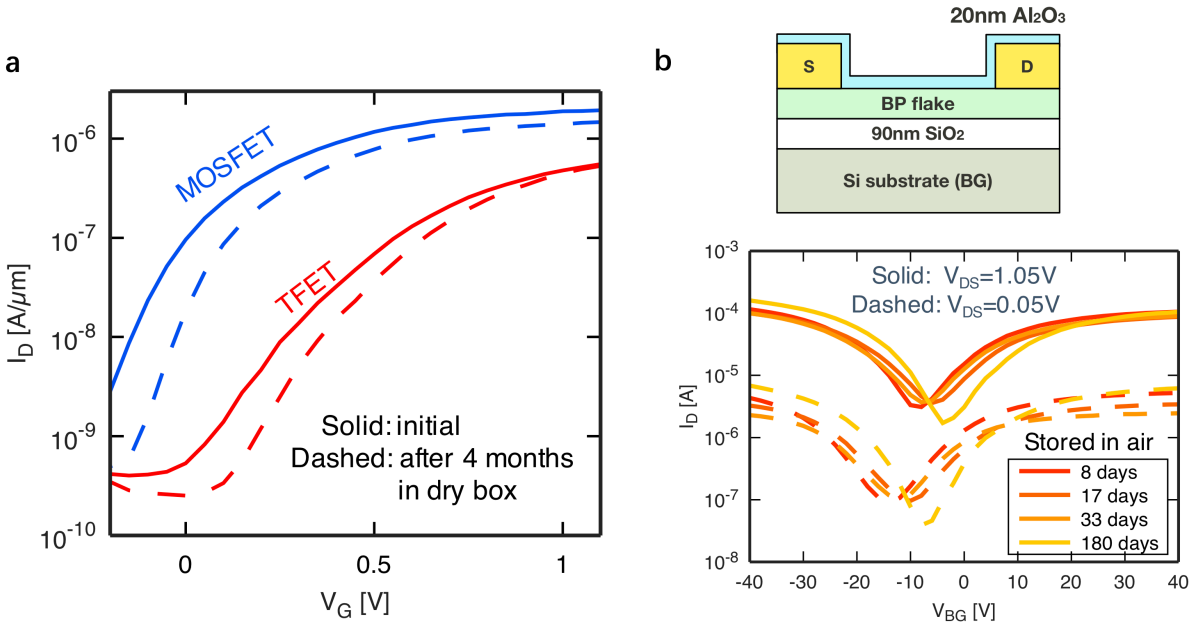

Figure S5. Stability of black phosphorus. (a) Comparison of transfer characteristics of the BP RED-TFET measured immediately after fabrication and after storage in an inert atmosphere for 4 months. No significant change is observed except for a shift in threshold voltage. (b) Transfer characteristics of a BP FET passivated by Al_2O_3. No significant changes are observed after storage in air for 180 days.

6. Effects of BP orientation and transport direction on BTBT

BP exhibits anisotropic effective masses along different transport directions.[8] DFT calculations[8] show that in monolayer BP, the carrier effective masses are 0.15 m_0 (holes) and 0.17 m_0 (electrons) in the armchair direction, and 6.35 m_0 (holes) and 1.12 m_0 (electrons) in the zigzag direction. On the other hand, in bulk BP, the values are 0.14 m_0 (holes) and 0.15 m_0 (electrons) in the armchair direction, and 0.71 m_0 (holes) and 1.15 m_0 (electrons) in the zigzag direction.

As we have discussed in the main text, the BTBT tunneling current is exponentially dependent on the effective mass. Therefore, the current level of a BP TFET depends on the transport direction. It has been experimentally demonstrated in ref [9] that the anisotropy of band-to-band tunneling in armchair direction and zigzag direction in BP can be up to 10^4. Here, we have investigated the effects of BP orientation on BTBT by both i) simulation and ii) a statistical study of experimental device currents.

Figure S6(a) shows the analytic modeling approach for the orientation-dependent BTBT current in BP TFETs. We have calculated a tunneling direction dependent transmission $T(\theta)$ based on the direction dependent tunneling distance $\lambda/\cos(\theta)$ and effective mass $m^*(\theta)$, and integrate over the full range of transport directions to obtain the total BTBT current I_{ON}. Considering the effective masses anisotropy in BP, the tunneling direction dependent effective mass $m^*(\theta)$ is estimated by assuming an elliptical iso-energy surface in k-space. Figure S6(b) shows the results of the model. The dependence of ON-current on the orientation of the BP device shows a strong non-linear behavior. However, while the possible range of I_{max}/I between transport in the armchair and in the zigzag direction can be as much as ~10^3, the ON-current differs only by less than 50% when the transport direction is within 30° of the armchair direction.

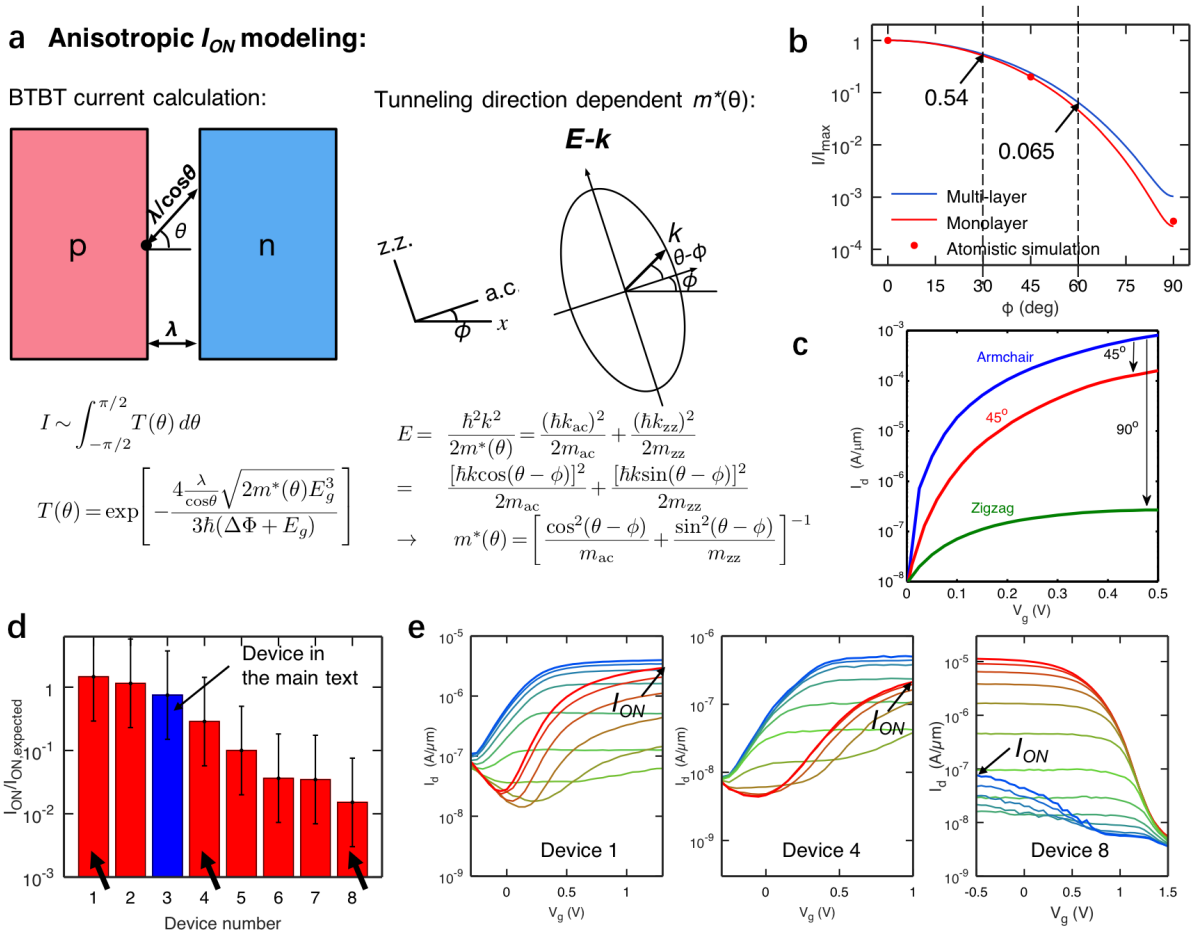

Figure S6. Effects of BP orientation and transport direction on BTBT. (a) Brief description of modeling approach of orientation-dependent BTBT current in BP TFETs. (b). Orientation-dependent I_{ON} of multi-layer and mono-layer BP TFETs from the model. The results match with atomistic simulation. (c) Atomistic simulation of effects of BP orientation on BTBT in a mono-layer TFET with EOT=0.5nm. (d) Statistics of I_{ON} of experimental devices, normalized by expected I_{ON}. (e) Exemplary device characteristics from the statistics in (d).

Figure S6(c) shows atomistic simulations of I_d-V_g curves for a BP TFET along different transport directions. The thickness of BP in the simulation is assumed to be that of a single mono-layer and the gate oxide is HfO_2 with an EOT = 0.5 nm with the spacer between separate gates etched away. This simulation has not been performed for the larger flake thicknesses since a reduced symmetry in the structure along the transverse direction significantly increases the computational cost, which makes it unfeasible to perform simulations with thicker cross-sections. This point can however be addressed by the analytic modeling approach shown in Figure S6(a). The atomistic simulation results match well with the analytical model, as shown by the red dots and line in Figure S6(b).

We have further investigated the effects of orientation on the ON-currents in BP TFET through a statistical study of our experimental data. In the experiments, the orientation of BP is not controlled deliberately; therefore, one can assume the orientation of BP to be randomly distributed between 0° to 90°. Figure S6(d) shows the statistical distribution of ON-currents of experimental BP TFETs, normalized by the "expected" ON-current values. The "expected" ON-current values are estimated from the body thickness of the BP flake, assuming that transport is

along the armchair direction. Note that since these devices share the same triple-gate structure, the main factors affecting ON-currents are the bandgap and the screening length λ, which can be deduced from the body thickness of the individual devices. In Figure S6(d) we assign an error bar of 5X to the expected ON-current, considering the uncertainty in body thickness estimation. One can see that the distribution matches approximately with the orientation-dependent trend from our analytic model shown in Figure S6(b). The device investigated in the main text, indicated by the blue bar, falls into the category of less than 50% deviation from the armchair direction, *i.e.*, the transport direction is expected to be within 30° of the armchair direction. However, the eight devices explored by us cover indeed the expected range of ON-currents for differently oriented BP TFETs. In order to control the orientation of BP more precisely, one could envision determining the orientation of BP using angle-dependent Raman spectroscopy prior to device fabrication and alignment of the channel in the armchair direction.[9]

Figure S6(e) shows exemplary device characteristics of the devices indicated by the black arrows from the statistical study shown in Figure S6(d). It is worth mentioning that in Device 8, the BTBT branch is already barely observable, since the thermal current cut-off limit at room-temperature is only less than one order of magnitude lower. This implies that a device with $I_{ON}/I_{ON,expected}$ below 10^{-2} may yield a BTBT branch that is not observable at all, which is likely the reason why lower currents as predicted by Figure S6(b) were not observed in Figure S6(d).

7. Scaling of vertical and lateral TFETs

Figure S7 shows a qualitative comparison of the scaling properties of a vertical TFET and a lateral TFET. One can easily see that since the tunneling area in a vertical TFET is proportional to the channel length L, the normalized ON-current will decrease proportionally when scaling down the channel length, as shown in Figure S7(a). Moreover, the accessible steep slope regime will also decrease after scaling. By contrast, the ON-current of a lateral device will not be affected by channel length scaling, as shown in Figure S7(b). Therefore, lateral TFETs have better scaling potential than vertical TFETs.

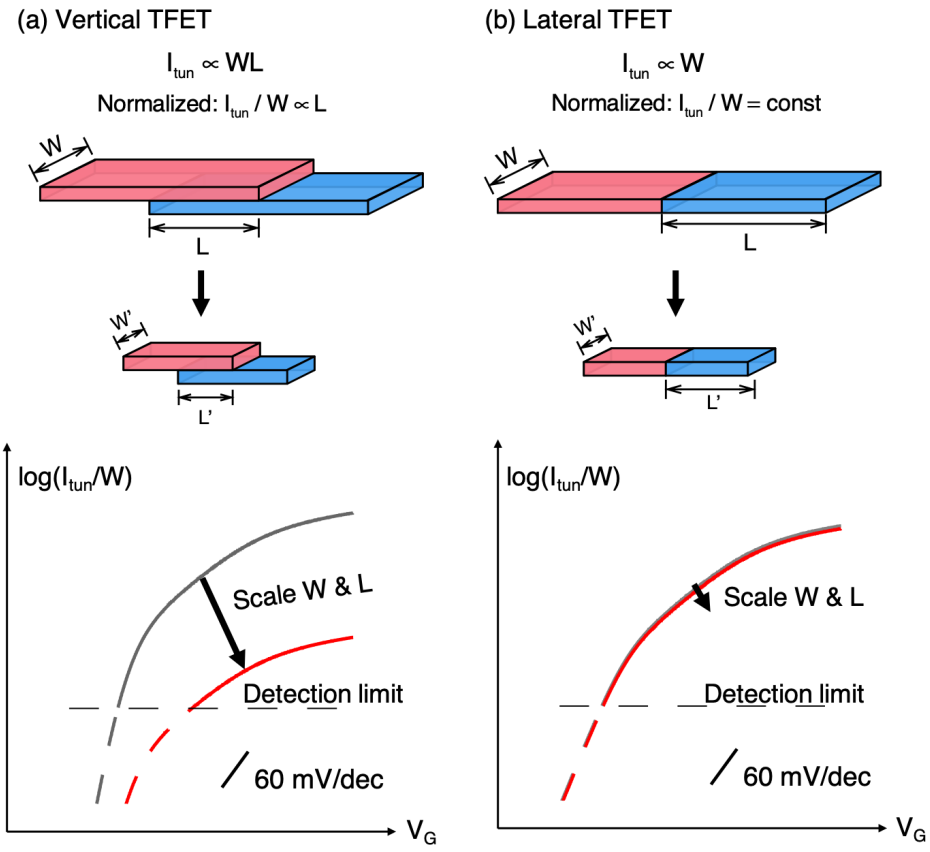

Figure S7. Comparison of scaling for (a) a vertical TFET and (b) a lateral TFET

8. Device structure and characteristics of an earlier prototype device

Figure S8 shows the device structure and characteristics of an earlier prototype device (denoted as "Exp. 2" in Figure 5a in main text). Figure S8(a) shows the schematic and SEM image of the device. The device structure is similar to the BP RED-TFET in the main text, except that the dielectric is composed of a 1.2 nm SiO_2/5 nm Al_2O_3 stack, instead of the HfO_2/Al_2O_3 stack in the main text. Figure S8(b) shows an AFM image and a line scan of the BP flake used for the device, showing an apparent thickness of t_{body}=12.8 nm. According to the analysis in the Supplementary Section 1, the PO_x formation means that this device has a real body and oxide thickness of t'_{body}=7 nm and t'_{ox}=8.1 nm, numbers that were used in the simulation shown in Figure 5a. Figure S8(c, d) show the transfer characteristics of the device in n-type and p-type configurations, respectively. By tuning the source or drain doping conditions, transitions from the MOSFET modes to the TFET modes are observed. Figure S8(e, f) shows the band diagrams of the device in the n-type and p-type configurations, showing the transitions from the MOSFET modes to the TFET modes.

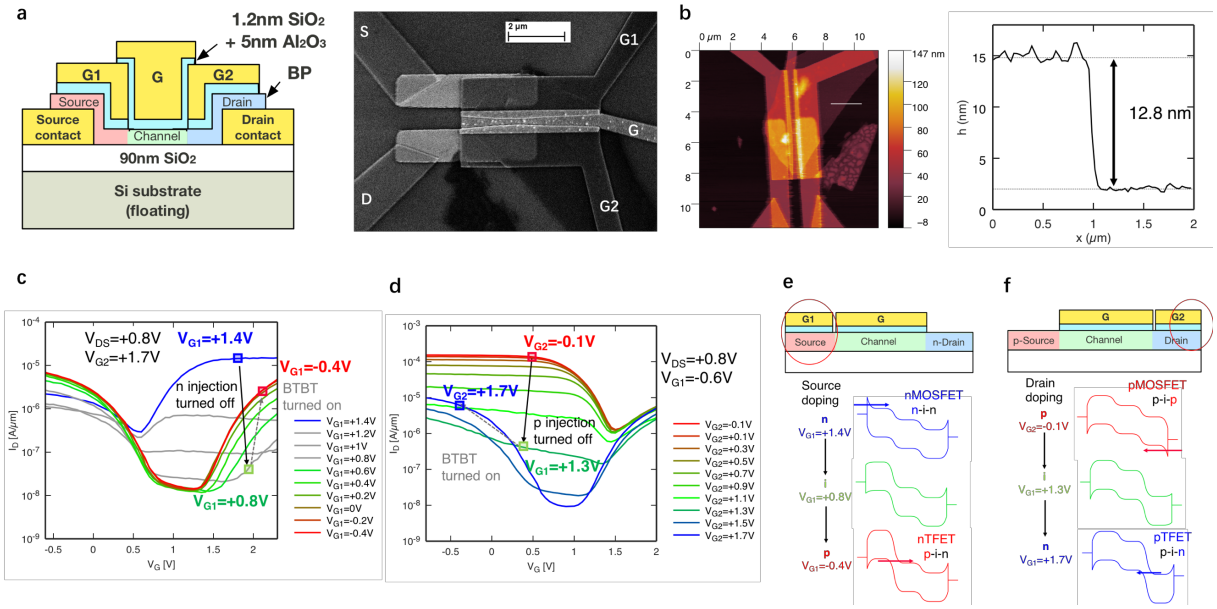

Figure S8. (a) Schematic and SEM image of an earlier prototype device (Exp. 2 in Figure 5). (b) AFM image and line scan of the BP flake, showing an apparent BP thickness of 12.8 nm. (c, d) Transfer characteristics of the device in (c) n-type and (d) p-type configurations under different (c) source (d) drain doping conditions, showing the transition from the MOSFET mode to the TFET mode. (e, f) Band diagrams of the device in (c) n-type and (d) p-type configurations corresponding to different source or drain doping conditions.

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