Supporting Information

Ultrafast Nanoscale Phase-Change Memory Enabled By Single-Pulse Conditioning

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Experimental and Modelling Methods

System Structure. Figure 1e shows the structure of a phase-change memory system which was deposited on a SiO_2-on-Si substrate, based on our previous device configuration.[S1] The system has a pore-like structure comprising a 20 nm-thick $Ge_2Sb_2Te_5$ layer, which was sandwiched between 200 nm-thick top and bottom TiW electrodes. The GST–225 was confined in the 5 nm–1 μm-wide pores formed by the 20 nm-thick SiO_2 insulating layer. The electrodes were used to connect the test structure to the external circuitry for electrical measurements, while the silica insulator provides electrical and thermal insulation.

Structure Fabrication. The chalcogenide systems were fabricated using an integrated conventional lithography and nano-patterning technique, according to our previous fabrication protocol.[S1] Each patterning step was accomplished using 365 nm photolithography (Cannon) or electron-beam lithography (JEOL), followed by the materials deposition and lift-off processes. All of the materials were deposited using composite targets in a DC magnetron sputtering system (Balzers Cube). A 4" Si wafer with a 1 μm-thick SiO_2 layer was used as the starting configuration, on which a 200 nm-thick TiW bottom electrode was deposited and patterned. An insulating layer, comprising a 20 nm-thick layer of SiO_2, was deposited and etched to form pores with diameters between 5 nm–1 μm. The openings were filled with a 20 nm-thick layer of $Ge_2Sb_2Te_5$ to form the active region. Finally, a 200 nm-thick TiW top electrode was deposited to complete the system structure.

Material Characterization. The GST–225 film was deposited using DC magnetron sputtering of a composite $Ge_2Sb_2Te_5$ target in a Balzers Cube sputtering system. The GST layer was characterized using X-ray photoelectron spectroscopy (ESCALab & Thetaprobe), and the concentrations of Ge, Sb and Te were 23.9 at%, 25.3 at% and 50.8 at%, respectively. The PCM structure was imaged using a transmission electron microscope (TEM) (FEI Tecnai) at 120 kV, and an atomic force microscope (AFM) (Veeco Dimension) under ambient conditions (Supporting Information Figure S1). Previous studies have demonstrated structures with pores on the order of a nanometre length scale using atomic force microscopy.[S2] Similarly, the current work also showed a system with nanometre-scale openings using an atomic force microscope.

Electrical Measurements. The structure was probed using a custom-built PCM-characterization system comprising a picosecond (Picosecond Pulse Labs) or nanosecond (Tektronix) pulse generator, a digital oscilloscope (Agilent Technologies) and a probe station, based on our previous measurement protocol[S1] (Supporting Information Figure S1). The picosecond pulse generator has the specifications of pulse durations ranging from 100 ps to 10 ns, rise time of 65 ps, and maximum amplitude of 7.5 V, and the nanosecond pulse generator has the specifications of pulse durations varying between 5-900 ns, a rise time of less than 3 ns, and a maximum voltage amplitude of 5.0 V. The system is connected to the pulse generator and oscilloscope via low-capacitance cables (~0.2 to 3 pF) and a load resistor of $R_l = 50\ \Omega$. The upper limit of the time constant of the resistance-capacitance circuit is estimated to be several 10 ps. The FWHM time duration

of the pulse was measured at V_A, and this was used to characterize the times of switching in the structures. We have previously investigated and reported the waveform of the voltage pulses obtained at V_A and V_B.[S1] As in those studies, the waveform of the pulse obtained at V_A also reflects the exact voltage pulse that is applied to the system, taking into account the capacitance or inductance of the probe, circuitry, and connectors. The FWHMs of the waveforms measured at V_A and V_B are almost the same. In addition, as the signal measured at V_B has passed through the structure, the duration of the pulse experienced by the system is almost identical to that of the pulse entering the configuration. Furthermore, a comparison of the shapes of the pulses measured at V_A and V_B also shows that parasitic-capacitance effects in the circuit or structure are negligible (see Figure 1d), and, in the case where they do exist near the end of the pulses, they dissipate in a time with an upper limit of a few nanoseconds, consistent with those reported by other groups.[S3,S4] We have used one of the conventional system structures used by many other research groups.[S5] The voltage-pulse duration needed to switch the large system using our present structure was found to be several tens of nanoseconds (depending on the voltage applied; see Figure 2g), which is about the same as those achieved with other system configurations.[S6] The duration and height of the voltage pulses were varied from several 100 ps to several 10 ns, and from 0 V to 7 V, respectively. To ensure good functionality, the structures were switched reversibly more than 100 times between the low-resistance level of about 10 kΩ and the high-resistance level of about 300 kΩ before the experimental study. The occurrence of crystallization was determined by the change of the resistance level of structure. The resistance change

of structure with small pore size was of a 'sudden-drop' type and the structure with large pore size showed similar behaviour. This is because the structures used the same active material (Supporting Information Figure S3). The resistance of the amorphous state is lower than the typical range of about 1 MΩ. This is because a small system size and a thin phase-change layer were used. The amorphous region would be smaller, and hence the resistance of the amorphous state is lower.

The crystallization process is slower than amorphization and it represents the switching-time limitation of phase-change systems. This time limitation of PC systems has been previously studied. In that work, the origin of the time limitation can be divided into two contributions: 1) crystal-nucleation limitation; and 2) crystal-growth limitation. The maximum crystallization rate of phase-change systems is determined by the total rates for nucleation (Eqn. 1) and growth (Eqn. 2)[S7]:

$$I(t) = 4f(1)\gamma n_c^{2/3} Z \exp\frac{16\pi v_m^2 \sigma^3}{3\Delta g^2 k_B T}\left(\frac{4\pi\tau}{t}\right)^{1/2} \exp\left(-\frac{\pi^2\tau}{4t}\right) \quad (1)$$

where $f(1)$ is the concentration of GST molecules, Z is the Zeldovich factor, γ is the molecular jump frequency at the interface between amorphous and crystalline phases, n_c is the maximum number of GST molecules in the cluster, v_m is the volume of a GST 'molecule', σ is the interfacial energy, Δg is the bulk free-energy difference per GST molecule between amorphous and crystalline phases, k_B is the Boltzmann constant, T is

the temperature, τ is the rate of molecular rearrangements during nucleation, and t is the time.

$$\frac{dr}{dt} = \frac{16D}{\pi^2}\left(\frac{3v_m}{4\pi}\right)^{1/3} \sinh\left[\frac{1}{2k_BT}\left(\Delta g - \frac{2\sigma}{r}v_m\right)\right] \quad (2)$$

where D is the diffusional jump frequency of GST molecules, v_m is the volume of a GST molecule, k_B is the Boltzmann constant, T is the temperature, Δg is the bulk free-energy difference per GST molecule between amorphous and crystalline phases, σ is the interfacial energy and r is the radius of a cluster.

The maximum crystallization rate of the GeSbTe and GeTe systems has been analyzed based on the above equations, and the time has been shown to be approximately faster than the duration of the shortest pulse used for full crystallization.[S8,S9] The same (GeTe) research group has previously shown an estimate of the minimum crystallization time for GeTe of about 1 ns.[S10] The current group has also demonstrated a similar estimate of the minimum crystallisation time for GST of ~500 ps.[S11] We note, however, that an accurate estimation of the maximum rate is still limited because the interfacial energy is generally difficult to obtain from experiments, especially for the metastable rocksalt phase of the phase-change materials.

Thermal Analysis. The structure was characterized using a custom-built PCM resistance-measurement system, based on our previous testing methodology.[S12] The setup consisted of a thermal-chuck system (Micromanipulator), hot plate and multimeter (Keithley). The thermal-chuck system controls the temperature of the hot plate, while the multimeter records the electrical resistance of the configuration. The structure was placed on a hot plate and annealed at temperatures varying between 300 K and 500 K, with the resistance level of the structure being recorded simultaneously using the multimeter. The configuration was initially at a high-resistance level (about 300 kΩ).

Finite-Element-Method Simulations. The temperature-distribution calculations were carried out by finite-element methods (FEM) using the ANSYS software, according to our previous simulational protocol.[S13] To study the excitation dependence of thermal diffusion, we have chosen to use a model configuration comprising a 40 nm-thick $Ge_2Sb_2Te_5$ layer sandwiched between 40 nm-thick TiW top and bottom electrodes. The GST–225 layer was also surrounded with a 40 nm-thick SiO_2 insulating layer. The values of the density, specific heat and thermal conductivity of SiO_2 were chosen to be 2650 kg m^{-3}, 1170 J kg^{-1} K^{-1} and 1.4 W m^{-1} K^{-1}, respectively, while the corresponding values for GST–225 were 6000 kg m^{-3}, 202 J kg^{-1} K^{-1} and 0.35 W m^{-1} K^{-1}, respectively, being intermediate between the values for the crystalline and amorphous phases.[S13,S14] The corresponding values for TiW were selected to be 14800 kg m^{-3}, 137 J kg^{-1} K^{-1} and 21.7 W m^{-1} K^{-1}, respectively.[S13,S14] Furthermore, to investigate the interface dependence of the thermal diffusion, the thermal resistance at the interface between SiO_2 and GST–225 was chosen to be between 10^{-8} and 10^{-10} W m^{-2} K^{-1}, in agreement with other studies.[S15] Heat

transfer was modelled using the heat-conduction equation with heat generation, which is characterized by the Joule heat generated per unit volume per unit time, Q, temperature, T, time, t, density, ρ, specific heat, c, and thermal conductivity, k, expressed as[S13]

$$\nabla \bullet k\nabla T + Q = \rho c \frac{\partial T}{\partial t} \tag{3}$$

The thermal distribution of the model was calculated for different applied voltages, and the material properties were assumed to be independent of temperature.

Additional Electrical and Modelling Data

Conventional System

The upper and lower crystallization voltage limits of the conventional structure for full crystallization were about 1.0 V and 0.6 V, respectively, in accordance with previous studies (albeit at lower voltage values) (Figure 2a).[S16] The conventional structure without pre-treatment could also, for example, under the application of a pulse of around 4 ns, crystallize with a voltage of ~0.85 V, in contrast to the structure with pre-treatment, which could crystallize with a voltage of approximately 0.75 V. Namely, this is about a 25% lower voltage value for an increase in pre-treatment under normalized crystallization voltage-limit conditions (((0.85 V − 0.6 V) − (0.75 V − 0.6 V)) × 100 / (1.0 V − 0.6 V)). This is important for the reduction of the overall crystallization energy (see Detailed Electrical and Calculation Analysis in Supporting Information). The time-dependent resistance drift for the amorphous phase was also reduced with an increase in pre-treatment, viz. drift coefficients, ν, of around 0.102 and 0.117 for the systems with and without pre-pulses, respectively (Figure 2e). For instance, this is about a 12.4% lower ν value for an increase in pre-treatment. Notably, the configurations with pre-pulsing showed a pore-size-dependent crystallization time, as manifested by the smaller the pore sizes, the shorter the voltage pulses required (Figure 2f). In addition, the endurance of the glassy state was unaffected, viz. a negligible change in the crystallization temperature for 10^6 and 10^4 cycles for configurations with and without pre-pulsing, respectively (Supporting Information Figure S2b). The crystalline-to-amorphous transition time, viz. with ~500 ps pulses, was also observed to be unaffected, while achieving rapid crystal

nucleation and growth via pre-pulsing (Supporting Information Figure S2c). In addition, Supporting Information Figure S2d demonstrates theoretical calculations showing that the higher the thermal boundary-resistance values, for instance at the SiO_2-$Ge_2Sb_2Te_5$ interface, the higher the peak-temperature values required for rapid nucleation and growth, in agreement with Figure 2a. Since pre-treatment often creates crystalline structures around an amorphous mark,[S17] this yields a higher number of interfaces between each layer inside GST–225 in the amorphous and crystalline phases compared to, for example, the bare amorphous GST–225 phase, resulting in a higher thermal boundary-resistance value.[S18]

Stackable System

Figure 2g shows a plot of the voltage as a function of the pulse length needed for crystallizing a system with a stacked configuration with and without pre-pulsing. SiO_2-on-Si was used as the starting structure, on which a 200 nm-thick TiW bottom electrode was patterned, followed by the formation of a 20 nm-thick phase-change layer and a 20 nm-thick switching layer inter-linked by a 5 nm-thick TiW layer, and capped by a 200 nm-thick TiW top electrode. Detailed Electrical and Calculation Analysis in Supporting Information describes the design and functionality of the system. The measurement protocol is similar to the ones used in Figure 2a. It can be seen that systems without pre-treatment did not show structural ordering using a voltage-pulse duration below a nanosecond, in marked contrast to the pre-treated systems, which exhibited crystal nucleation and growth with a sub-nanosecond pulse, viz. 6 ns and 900 ps for a voltage level around 1.1 V for non-pretreated and pretreated systems, respectively, i.e. about six

times faster with an increase in pre-treatment. Stability of the system with a stacked configuration at a low-resistance level is often measured by the voltage at which the structure switches from the resistive off- to the conductive on-state during cycling.[S19] The voltage for switching the system from off- to on-states is also known as the threshold voltage, V_T, and the longer the structure can maintain similar V_T values, the higher the stability of the configuration.[S19] Note also that the rapid nucleation and growth was observed not to affect the stability of the pre-treated system in the low-resistance state,[S19] viz. V_T of around 0.4 V for 10^6 cycles (see Figure S4c and Detailed Electrical and Calculation Analysis in Supporting Information).

Multi-level System

We also observed fast structural ordering assisted by pre-pulsing in systems with multi-level configurations. A study of the control of crystal nucleation and growth is given in Figure 2h in terms of a plot of the resistance state as a function of different voltage pulses for varying pulse lengths. The structure used is similar to the configuration used for Figure 2a. The durations of the shortest voltage pulses needed for switching the systems between low-, intermediate- and high-resistance levels were measured. These results indicate that, unlike the structures without pre-treatment, which did not exhibit crystallization under the application of voltage pulses less than a nanosecond in duration, the pre-treated systems displayed crystal nucleation and growth following a sub-1 ns pulse. For example, pulse durations around 1.6 ns and 800 ps were exhibited for the non-pretreated and pretreated systems, respectively, for R values between 10 kΩ, 150 kΩ and 300 kΩ, i.e. about two times faster with an increase in pre-treatment. It is notable that this

was observed not to affect the time-dependent drift of the resistance levels, viz. drift power-law values, ν, were approximately 0.0083, 0.0692 and 0.1028 for pre-treated systems with $R \approx 10$ kΩ, 150 kΩ and 300 kΩ, respectively, in agreement with Figure 2e (see Figure S2a and Detailed Electrical and Calculation Analysis in Supporting Information).

Detailed Electrical and Calculation Analysis

Conventional and Multi-Level Systems

Energy for pre-treatment. The energy needed to pre-treat the configurations can be estimated by a simple calculation of the sum of the square-voltage-amplitude-to-initial-resistance-level ratio and pulse-duration products, viz. $E = (V^2 / R)\, t$, based on previous melting studies.[S1] Phase-change systems are often used or cycled for more than a million times.[S20] Similarly, for instance, in a million cycles, a system with the single-shot treatment, e.g. a ~ 5.0 V–60 ns pre-pulse at an initial resistance level of about 300 k Ω, will also require overall less energy compared to the structure with multiple constant-low-voltage treatment,[S11] e.g. 10^6 cycles using a ~ 0.3 V–100 ns pre-pulse at an initial resistance level of around 300 kΩ. In the calculation, single-shot treated, E_o = (5.0 V^2 / 300 kΩ) × 60 ns ≈ 5 pJ; multiple constant-low-voltage treated, $E_o = 10^6 \times$ (0.3 V^2 / 300 k Ω) × 100 ns ≈ 30,000 pJ, indicating that the single-shot treatment approach can also significantly reduce the pre-treatment energy. In terms of the number of operations or implementation costs, for example, in a million cycles, a system with the single-shot treatment, e.g. a 5.0 V–60 ns pre-pulse, will also require a lower number of operations, n_o, than a structure with multiple constant-low-voltage treatment,[S11] e.g. 10^6 cycles using a ~ 0.3 V–100 ns pre-pulse. For the calculation, single-shot treated, $n_o \approx 1$; multiple constant-low-voltage treated, $n_o \approx 10^6$, meaning that the single-shot treatment method can also significantly reduce the implementation costs.

Overall crystallization energy. Previous studies have shown that systems with pre-treatment require a lower overall crystallization energy, compared to structures without pre-pulsing, for melting after multiple crystallization cycles.[S1] For our current work, the energy needed to crystallize the configurations can also be estimated by a simple calculation of the sum of the square-voltage-amplitude-to-initial-resistance-level ratio and pulse-duration products, viz. $E = (V^2 / R)\, t$, based on previous melting studies.[S1] Phase-change systems are often used or cycled for more than a million times.[S20] Similarly, for instance, in a million cycles, a system with pre-treatment, i.e. a ~ 5.0 V–60 ns pre-pulse and 10^6 cycles of around 0.75 V–4 ns main pulse at an initial resistance level of approximately 300 kΩ, will also require overall less energy compared to the structure without pre-treatment, i.e. 10^6 cycles using ~ 0.85 V–4 ns main-pulse at an initial resistance level of around 300 kΩ. In the calculation, pretreated; E_o = ((5.0 V^2 / 300 kΩ) × 60 ns) + (10^6 × (0.75 V^2 / 300 kΩ) × 4 ns) ≈ 7.505 nJ, non-pretreated; $E_o = 10^6 \times$ ((0.85 V^2/ 300 kΩ) × 4 ns) ≈ 9.633 nJ, indicating that the pre-treatment approach can reduce the overall crystallization energy.

Resistance drift. The resistance drift of the amorphous state of a phase-change system is typically described using a power law for the time dependence of the resistance[S21]

$$R = R_0 \, (t / t_0)^{\nu} \qquad (4)$$

where R is the resistance level, t denotes the time, t_0 is an arbitrarily chosen zero time and R_0 is the resistance at $t = t_0$. The resistance drift of a configuration is characterised by the drift coefficient v, i.e. the stronger the drift, the higher the value of the exponent, v. The v value is observed to be low for prototypical chalcogenide systems,[S21] viz. for GST, $v \sim 0.1$.

In previous works, phase-change structures with similar resistance levels under different moderate voltage biases have demonstrated similar v values.[S21] Similarly, in our current work, chalcogenide systems of similar resistance levels for varying high-voltage pre-treatments also showed similar v values: for example, without pre-pulses, $v \approx 0.117$; with pre-pulses, $v \sim 0.102$ (see Figure 2e). The structures with multiple resistance levels subject to pre-pulsing also exhibited low v values (Supporting Information Figure S2a), in accordance with other multi-level studies without pre-treatment.[S21] These findings therefore indicate that resistance drift does not accelerate when pre-pulsing is used.

For a PC-array implementation, a group of PC structures with multiple-resistance levels are generally used to store information. However, resistance-drift effects tend to cause the distributions of the resistance levels or v values of the structures to shift from their initial positions after writing, and also to move further apart, thus increasing the average margin between the adjacent resistance levels over time. In addition, the spread of each distribution does not change appreciably with time. Although a reliable reading of the stored resistance levels for such PC structures can be achieved by using an adaptive writing scheme,[S21] through placing appropriate reference thresholds between the

distributions of the adjacent resistance levels, and adjusting such thresholds over time according to the shift of the resistance levels due to drift effects, the bit-error rate in the structures deteriorates over time. This is because the resistance-drift effect is a random process, and hence the increase in the resistance levels of each structure evolves in a stochastic manner. Hence, upon the writing of information, although the initial resistance levels of the structures are separated, some of the levels may shift closer together, and cross each other at some point in time.

To minimize the resistance-drift effects, a modular writing scheme for PC structures has been demonstrated. The concept underlying such a scheme lies in the fact that, in the majority of the cases, the relative order of the structures switched to different resistance levels does not change due to the drift behavior of a cell.[S21] In the modified writing scheme, information is written in the relative order of the resistance levels for the structures in a group that forms a so-called 'codeword'. In most cases, resistance-drift effects do not affect this ordering, and therefore information could be read correctly. By employing such a scheme, storage of 4 levels per structure with a raw bit-error rate of the order of 10^{-5} was achieved in an array of 200,000 structures and maintained for over 30 days after writing at room temperature, which is more than one order of magnitude lower than by using the former adaptive writing scheme.[S21] It should be noted that a reading error occurs when two R levels corresponding to two cells of the same codeword cross each other in the course of time, but as the codewords needed are usually short, i.e. a small number of cells in a group, such events are quite rare, giving rise to a low bit-error rate, although at the expense of some capacity loss. The present development of a low-

redundancy, error-correction code is expected to reduce further the overall error rate towards 10^{-15}, which is required for practical device applications. The resistance-drift effects can be further minimized via reducing the size of the PC material. Nanowire-based PC cells, for instance, show an extremely low v value due to the efficient stress relaxation from a larger exposed free surface compared with thin-film-based cells, although it would be more difficult to synthesize or fabricate these devices.[S22]

Overall, it has been shown that the resistance drift of a PC structure can be controlled and minimized accordingly, which would enable the integration of the PC structure with a Si transistor or a similar switching device, and the reliable reading of the information stored in a structure, respectively, although additional modifications may be required.

Data Retention. The data-retention duration of a phase-change memory structure is often measured by the isothermal change in the resistance level, based on the Arrhenius equation[S23]

$$t_c = \tau \exp (E_a / k_B T) \tag{5}$$

where t_c, τ, E_a, k_B, and T are the onset time of crystallization, a time coefficient, activation energy for crystallization, Boltzmann's constant and the temperature, respectively. The time, t_c, is defined by the time when the system switches from a high- to low-resistance level. Extrapolation of a fitted line of the crystallization time versus reciprocal temperature is used to estimate the maximum temperature, T_m, allowable to

retain data for 10 years, i.e. the higher the temperature, the shorter the retention duration of the data. The temperature for 10-year data retention is observed to be high for conventional PC chalcogenide systems, viz. for $Ge_2Sb_2Te_5$, T_m ~ 388 K.[S23]

In previous studies, different phase-change structures with similar resistance levels have shown similar maximum temperatures for retaining data for 10 years.[S23] Similarly, in our current work, chalcogenide structures with and without pre-treatments of similar resistance states also showed similar temperatures for 10-year data retention, viz. without pre-pulses, $T_m \approx 372$ K; with pre-pulses, T_m ~ 368 K (see Figure 2b), meaning that pre-pulsing can maintain a high level of data retention.

Endurance of the glassy phase. The endurance of the amorphous phase can be characterized by the onset number, after cycling, for a variation in crystallization properties.[S24] Previous studies have shown a higher crystallization or switching voltage with an increase in cycle number.[S24] Similarly, in the current study, a chalcogenide system with and without pre-pulsing also showed that, the higher the cycling number, the higher is the crystallization temperature (Supporting Information Figure S2b). Phase-change structures with pre-pulsing also displayed a higher onset in the number of cycles before a change in crystallization temperature was observed, showing that pre-treatment can enhance the endurance of the amorphous state.

Crystalline-to-amorphous transition time. It is believed that crystalline-to-amorphous phase transitions normally involve the melting of a system at high

temperatures, followed by rapid quenching of the configuration to the amorphous state.[S25] Fast crystal-to-glass transformations are typically achieved by short pulse lengths.[S25] In previous studies, phase-change structures without pre-treatment have exhibited rapid melting (and quenching), as caused by voltage pulses below a nanosecond.[S25] Similarly, in our current work, a chalcogenide system with pre-pulsing also showed that pulse durations of the order of hundreds of picoseconds can cause amorphization (Supporting Information Figure S2c), showing that pre-treatment can preserve quick melting and quenching.

Device downsizing. Reduction in the size of the amorphous region has been shown to produce a faster rate of crystallization in chalcogenide structures with GeTe.[S10] A quicker crystallization rate is often manifested by a shorter pulse duration to crystallize a system.[S10] Similarly, in our current work, a phase-change structure using GST–225 with pre-treatment also showed that, the smaller the size of the glassy region, the shorter the pulse duration needed for crystallization (see Figure 2f), indicating that pre-treatment can be compatible with device downscaling.

Pre-treatment-pulse-length-dependent crystallization time. Researchers have previously demonstrated a shorter crystallization-pulse duration with an increase in pre-treatment-pulse duration using optical pulses.[S26] The current paper has also exhibited shorter-duration crystallization pulses, e.g. around 400 ps, with a similar increase in pre-treatment-pulse duration, meaning that the rate of crystallization can be enhanced via an increase in pre-treatment.

Theoretical calculations. Theoretical calculations also reproduce the higher thermal confinement facilitated by pre-pulsing for reducing power consumption. Phase-change systems, for instance, have shown a higher thermal-resistance value at the interface between SiO_2 and $Ge_2Sb_2Te_5$ for an increase in the number of interfaces between each layer inside GST–225 in amorphous and crystalline phases.[S18] In optical studies, GST–225 with pre-treatment has shown crystalline structures surrounding an amorphous mark,[S17] indicating that it has a higher number of interfaces compared to, for example, the bare amorphous GST phase. A higher degree of thermal concentration is often concomitant with a higher peak temperature in the chalcogenide system.[S27] Based on these studies, we similarly investigate the interface dependence of the peak temperature for the phase-change system. The structure showed a higher peak temperature with an increase of thermal resistance at the SiO_2–$Ge_2Sb_2Te_5$ boundary (Supporting Information Figure S2d), indicating that systems with pre-pulsing should have a higher thermal confinement. The rate of crystal nucleation peaks at lower temperatures, while that for crystal growth peaks at higher temperatures.[S28] A system with an overall high peak temperature or under pre-treatment conditions should also yield rapid crystal nucleation and growth.

Stackable Systems

Systems of stacked-type for 'cross-point' chalcogenide arrays often consist of a top electrode, selector layer and a phase-change layer interlinked by metal, and a bottom electrode.[S19] The top and bottom electrodes are used to connect the structures to external

circuitry, while the selector layer acts as an electronic temporary switch selectively to access the phase-change layer upon the application of a suitable bias voltage. The PC layer can store the data bits ‘1’ and ‘0’ permanently, while the metal can serve as a barrier layer. Selector layers often remain at higher resistance levels, while the phase-change layer can be altered from high- to low-resistance levels.[S19] In a cross-point array, to select a structure, a voltage bias is applied to the selected column and row. The structure is accessed by the selector, which can be switched to access the phase-change layer. The system typically shows a threshold-switching behavior, whereby the structure shows switching from resistive off- to conductive on-states at a threshold voltage, V_T. Disturbance of an adjacent system is avoided when the voltage drop at the structure is below the V_T values of the configuration with a low-resistance level.

Similarly, in our current work, we have also used structures with a stacked configuration for cross-point phase-change arrays. The system, for example, consists of a 200 nm-thick TiW top electrode, a 20 nm-thick doped-alloy selector layer (under patent) and a 20 nm-thick GST–225 chalcogenide layer interlinked by a 5 nm-thick TiW barrier layer, and a 200 nm-thick TiW bottom electrode. The structures also have a pore-like configuration, and the diameter of the pore was kept constant (about 35 nm). The structure can also be altered reversibly between high- and low-resistance levels, viz. around 350 kΩ and 190 kΩ, respectively, and the resistance levels are higher due to the high resistance of the selector layer. Structures with a low-resistance level under pre-treatment also showed threshold-switching behavior, and in the low-resistance level, the

phase-change layer and selector layer exhibit mostly crystalline and amorphous regions, respectively (Supporting Information Figures S4a,b).

The stability of a system with a stacked configuration at a low resistance level is usually measured by the voltage at which the structure switches from the resistive off- to the conductive on-state during cycling.[S19] The voltage for switching the system from off- to on-states is also known as the threshold voltage, V_T, and the longer the structure can maintain similar V_T values, the higher the stability of the configuration.[S19] In previous studies, a system with a stacked structure without pre-pulsing has already demonstrated almost constant V_T values for more than 10^6 cycles.[S19] Similarly, in this current work, a structure of stacked-type with pre-treatment also showed consistent V_T values for more than 10^6 cycles (Supporting Information Figure S4c), showing that pre-pulsing can maintain a good stability of a system with a stacked configuration for a low resistance level.

Other Electrical Data

Perhaps most significantly, the systems with pre-treatment also show a low degree of crystallinity: this can be seen in a plot of the resistance level as a function of different voltages and for varying pulse durations (Figure 1b). A crystal-nucleus population whose size is smaller than the critical nucleation size, r_C, is often manifested by high resistance levels, while a cluster distribution size larger than r_C exhibits a low resistivity.[S16] The structures subjected to short or weak voltage pulses, viz. with negligible pre-treatment, can show populations of nuclei with sizes that are smaller than r_C, as corroborated by their still high resistance levels, viz. around 300 kΩ, while systems subjected to moderate and strong pulses, i.e. with pre-pulsing, can exhibit some nuclei population sizes larger than r_C, concomitant with the lower limits of the high-resistance values, e.g. ~260 kΩ, in agreement with Figure 2. Moreover, the creation of the low-crystalline state is robust to different structural sizes, material backgrounds, numbers of cycles and system configurations, as we explain in the discussion below. In spite of previous work to investigate systems with weak and prolonged voltage pulses in the case of $Ge_1Sb_2Te_4$,[S29] a study of the effect of strong, moderate pulses applied to GST–225 is not available.

Phase-change films with different mark sizes, material backgrounds, cycling numbers and mark configurations have already shown crystalline structures surrounding amorphous marks produced by optical pre-pulses with high amplitudes and moderate durations.[S17]

The films have also shown correlations between the material characteristics and the pre-treatments; for example, a higher electrical conductivity is achieved for systems with pre-pulsing compared to films without pre-excitation,[S30] a higher pre-treatment energy for an increase in mark size,[S31] and a lower pre-excitation energy for films with a partially amorphous structure than for systems with a pure glassy phase.[S26] Additionally, the films have exhibited robust material signatures, viz. preservation of crystallites around amorphous marks after material cycling.[S26]

Similarly, in our current work, the structures also showed tunable material signatures, such as a lower resistance value as the system is changed from negligible pre-pulsing configuration to pre-pulsing configuration, viz. ~300 kΩ and 260 kΩ for the systems with voltage values of around 5.0 V and 7.0 V, respectively (Supporting Information Figure S6), a higher voltage for pre-treatment (or inducing a reduction in the resistance value) for an increase in the size of the structure, viz. about 7.0 V and 8.0 V for systems with pore sizes of around 800 nm and 1 μm, respectively, from ~300 kΩ to 260 k Ω, a lower voltage for pre-pulsing (or rendering a decrease in the resistance value) as the configuration is changed from a higher initial-resistance level type to a lower initial-resistance level type, viz. around 7.0 V and 6.0 V for the systems with initial resistance levels of approximately 300 kΩ and 280 kΩ, from around 300 kΩ and 280 kΩ to 260 kΩ,

respectively, and stability of the crystallites for structures with pre-treatment upon extended structural cycling, viz. a resistance level of around 270 kΩ for 1,000 cycles.

We note that chalcogenide films with pre-treatment have already shown a consistent formation of crystalline structures around amorphous marks for varying configurations,[S31] and since the phase-change structures without pre-pulsing of other research groups have also shown similar switching times[S32] as the system without pre-treatment used in this current work (see Figure 2g), the formation of crystallites around glassy marks should not be arbitrarily affected by a difference in configuration, although the crystallization effects could be further investigated in varying structures in the future.

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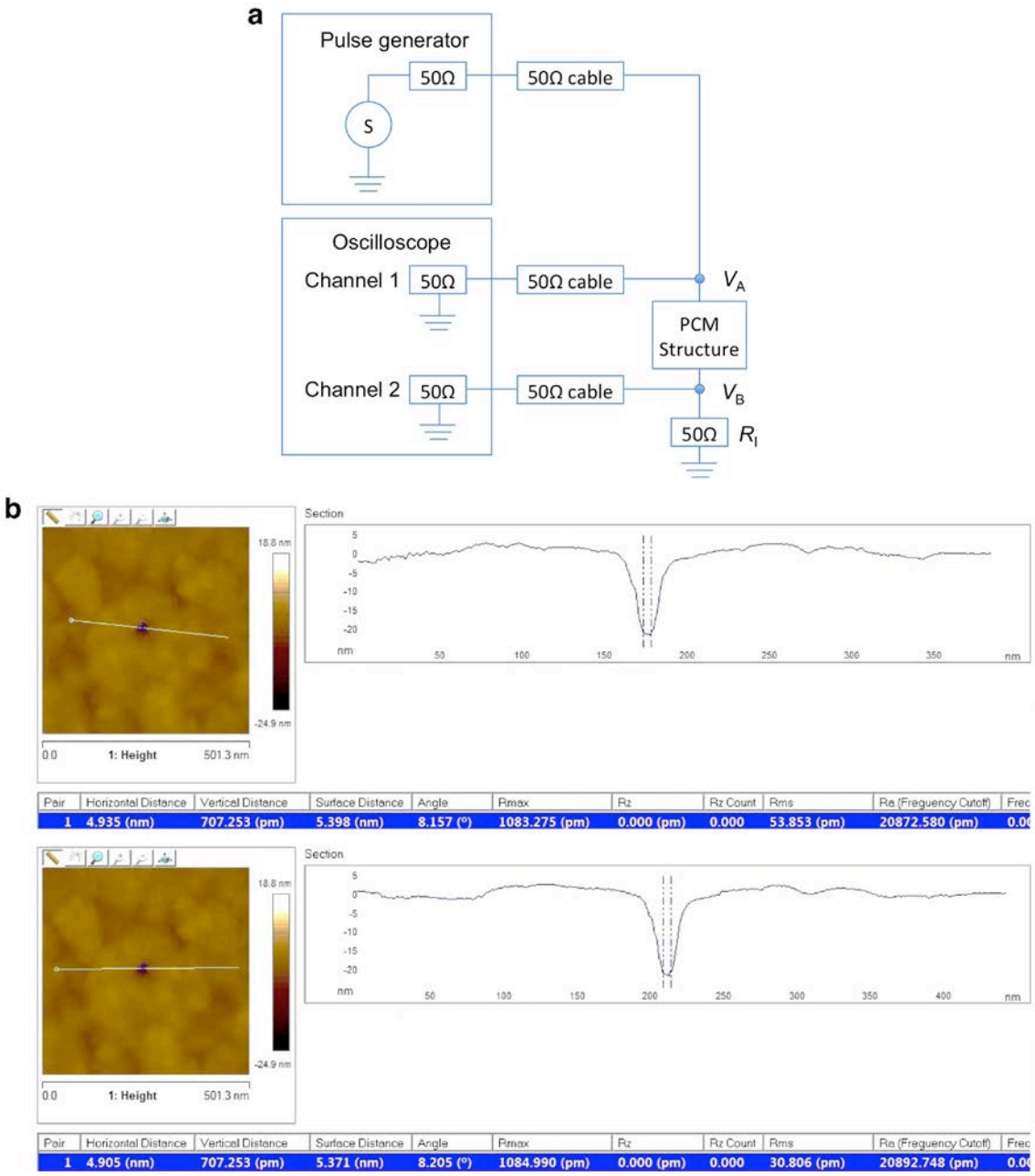
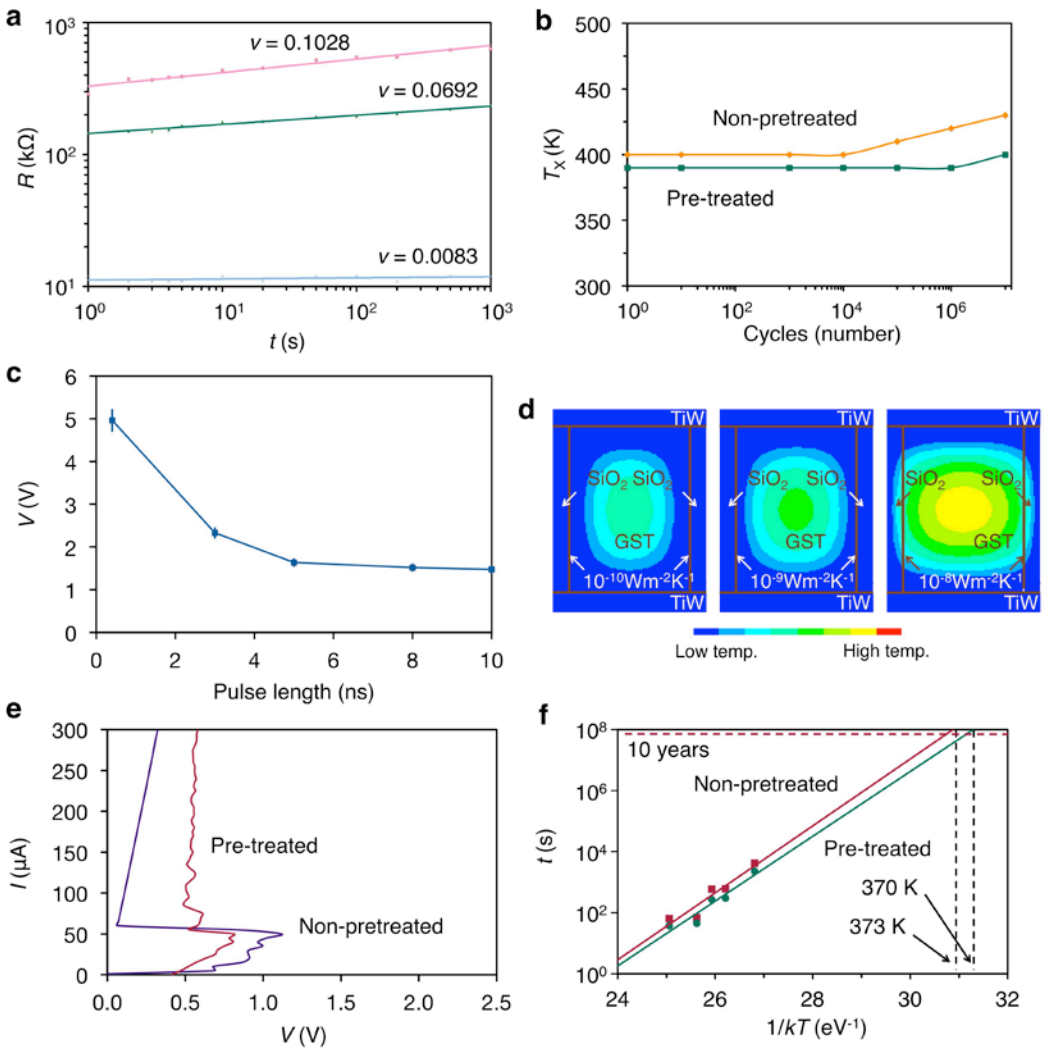
Figures

Figure S1



a) PCM measurement set-up. **b)** AFM images and surface profiles of the structural pores (along the white lines).

Figure S2



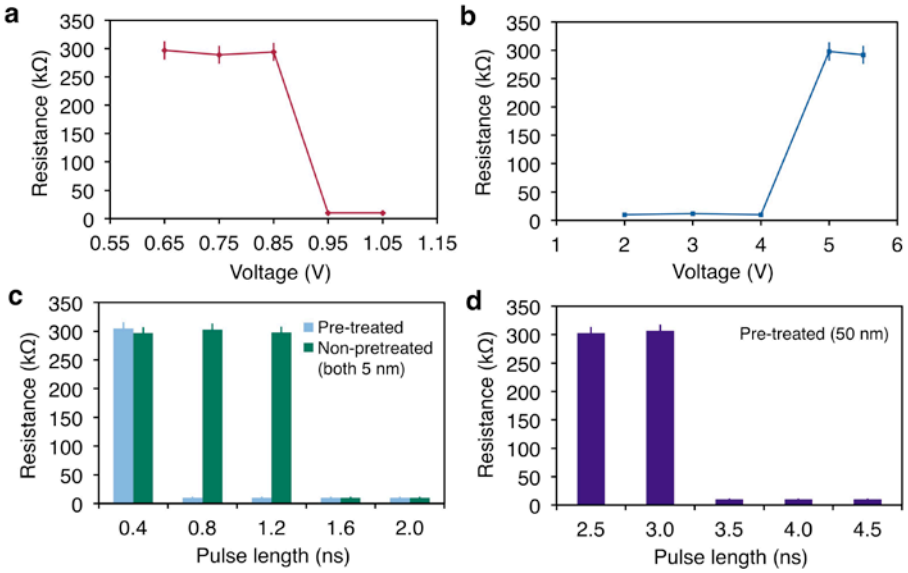
a) Time dependence (drift) of the resistance of the chalcogenide systems with different resistance levels under pre-pulsing. *v* is the resistance-drift coefficient of the structure, which is determined by a fit to a power law of the drift data, and the ambient temperature was maintained to be the same (around 300 K). The initial low-, intermediate- and high-resistance levels of the structures were kept constant at around 10 kΩ, 150 kΩ and 300 kΩ, respectively. **b)** Plot of the crystallization temperature as a

function of the cycle number of phase-change structures with (green line) and without (orange line) pre-treatment with constant voltage pulses, e.g. low- to high-resistance levels, around 3.0 V, 10 ns; high- to low-resistance levels, about 1.0 V, 30 ns. The high- and low-resistance levels were kept constant at around 300 kΩ and 10 kΩ, respectively.

c) Correlation between the voltage-pulse amplitude and duration to switch the chalcogenide structures with pre-treatment from low- to high-resistance levels. The initial low-resistance level was kept constant at around 10 kΩ. The error bars show the range of values obtained from experiments carried out on three different structures. **d)** Simulated temperature-contour plots of the phase-change systems with varying values of the thermal-boundary resistance at the SiO_2-GST interface. The voltage-pulse amplitude and duration were kept constant, and the initial temperature was kept constant at about 300 K. The material properties were chosen to be independent of temperature. **e)** *I*-*V* plot of the phase-change structures in a high-resistance level with (red line) and without (purple line) pre-pulsing for a constant pore size of the system (~300 nm). **f)** An Arrhenius extrapolation for 10-year data retention (of the amorphous state) of the prototypical structure with (green line) and without (red line) pre-pulsing. Detailed Electrical and Calculation Analysis in Supporting Information describes the measurement and calculation protocols. The structure was initially in the high-resistance level (~300 kΩ).

The voltage amplitude and duration of the pre-pulses for (a, b, c, e, f) were kept constant at about 5.0 V and 60 ns, respectively, and the pore size of the structure for (a, b, c, f) was maintained to be the same (around 5 nm).

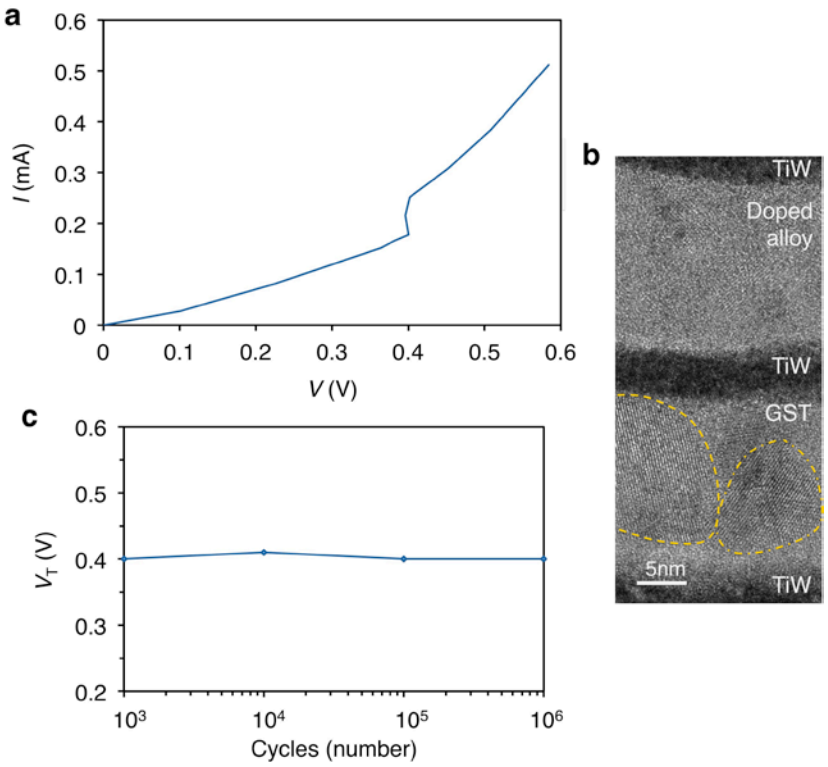
Figure S3



a) Dependence of the resistance level on the voltage required to switch the phase-change structure with pre-treatment from a high- to low-resistance level under a pulse duration of 900 ps. **b)** Correlation between the resistance level and voltage to switch the structure with pre-treatment from a low- to high-resistance level under a pulse duration of 600 ps. The pore size of the structure was maintained to be the same (approximately 5 nm). Plot of resistance as a function of pulse duration to switch the phase-change structure **c)** with and without pre-treatment and using 5-nm pore configuration, and **d)** with pre-treatment and using 50-nm pore configuration, from a high- to low-resistance level. The voltage-pulse amplitude was kept constant at approximately 1.0 V. For (a-d), the initial high- and low-resistance levels were kept constant at around 300 kΩ and 10 kΩ , respectively. The error bars show the range of values obtained from experiments carried out on three different structures. The structure with pre-treatment was subjected to a

voltage pulse (around 5.0 V, 60 ns) in a single-pulse conditioning, while the non-treated system remained untouched.

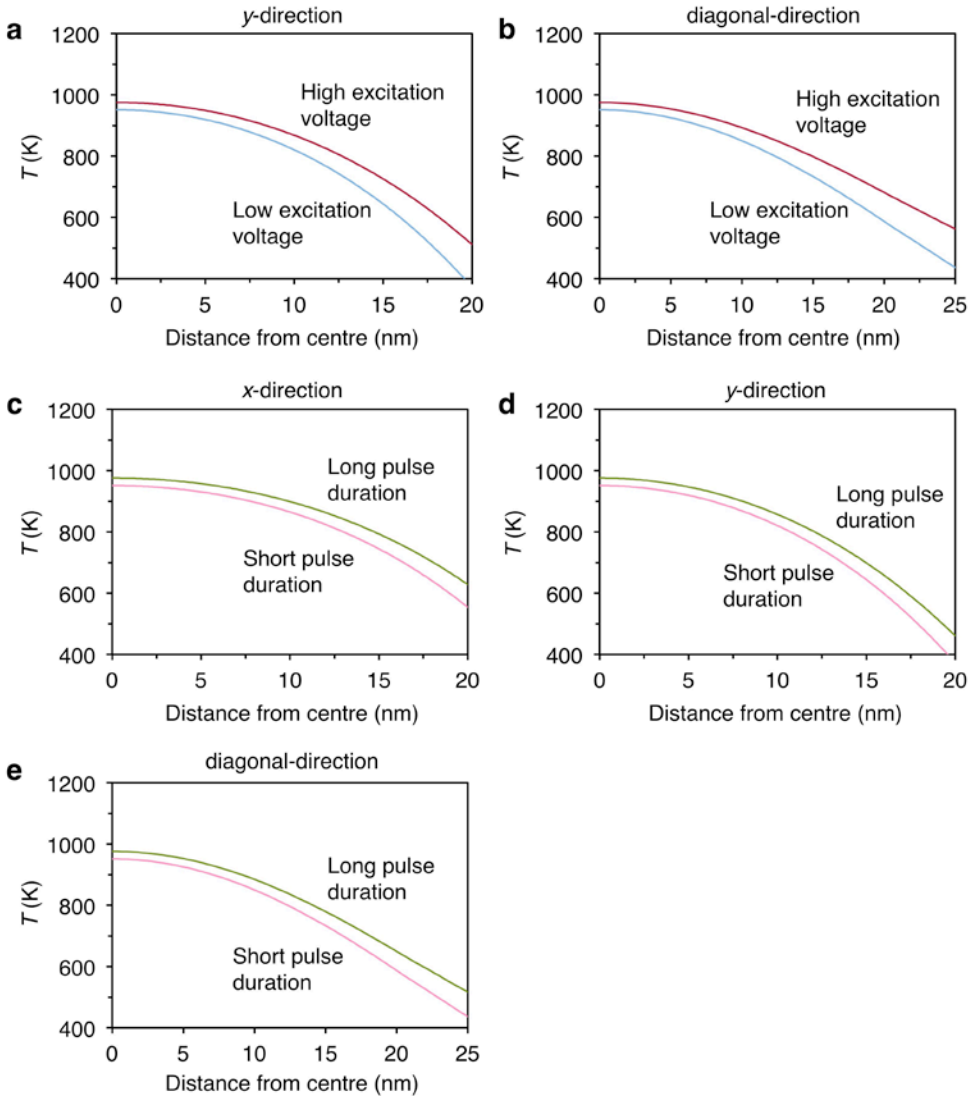
Figure S4



I-V plot **a)** and TEM image **b)** of the chalcogenide structure with a stacked configuration with pre-pulsing at a low-resistance level. The resistance level was kept constant at around 190 kΩ. The yellow dotted regions indicate the crystalline regions. **c)** Plot of the threshold voltage, V_T, as a function of the number of cycles for PCM structures with a stacked configuration under pre-treatment at a low-resistance level. The V_T values were obtained by measuring the voltage at which the structure switches from the resistive off- to conductive on-states. The structure was cycled between the high- and low-resistance levels of around 350 kΩ and 190 kΩ, respectively, and the cycling pulses were maintained to be the same, e.g. low to high resistance level, about 3.0 V, 10 ns; high to low resistance level, around 1.1 V, 50 ns. For (a-c), the voltage-pulse amplitude and

duration for the pre-treatment were kept constant at about 5.0 V and 60 ns, respectively. The pore size of the structure was maintained to be the same (~35 nm).

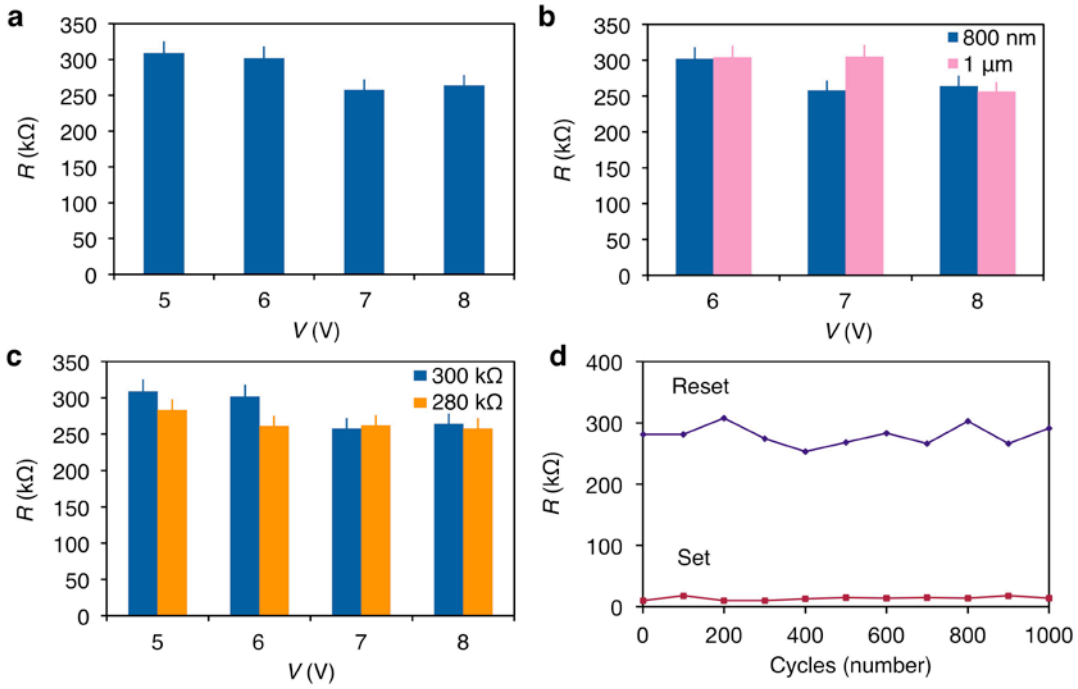
Figure S5



Simulated temperature-profile plots of the $Ge_2Sb_2Te_5$ layer of phase-change structures with high (red line) and low (blue line) excitation voltages along: **a)** the *y* direction; and **b)** diagonal directions. The pulse duration was kept constant, and the structures were excited by high (around 5.0 V) and low (~3.0 V) excitation voltages, respectively. Calculated temperature-profile plots of the GST–225 layer of the chalcogenide systems with moderate (green line) and short (pink line) pulse durations

along: **c)** the *x*-axis; **d)** the *y*-axis; and **e)** diagonal axes. The voltage was maintained to be the same, and the systems were excited via moderate (approximately 30 ns) and short (~5 ns) pulse durations, respectively. The initial temperature was kept constant (around 300 K), and the material properties were chosen to be independent of temperature. The *x*-direction is defined as being from the centre of the $Ge_2Sb_2Te_5$ layer to the right end of the layer, while the *y*-direction is defined as being from the centre of the GST–225 layer to the top end of the layer. The diagonal direction is defined as being from the centre of the GST layer to the top-right corner of the layer.

Figure S6



a) Dependence of the system resistance on the pulse voltage applied to the phase-change structure at high-resistance levels. **b)** Correlation between the resistance and the voltage applied to the chalcogenide system with different pore sizes. **c)** *R*-*V* plot of the phase-change structure for varying initial resistance levels. **d)** Plot of the resistance level as a function of the number of cycles to switch a chalcogenide structure with pre-pulsing between the high- ("reset") and low- ("set") resistance levels. The pulse voltage and pulse duration of the pre-treatment were kept constant (~7.0 V and 80 ns), and the "reset" and "set" pulses were maintainted to be the same, e.g. around 4.0 V–50 ns and 2.0 V–90 ns, respectively. The initial resistance levels of the structure for (a-b) were kept constant (around 300 kΩ), and the pulse duration was maintained to be the same (~70 ns). The error bars show the range of values obtained from experiments carried out on three

different structures. The size of the pore of the structure for (a, c, d) was kept constant (~800 nm).