Supporting Information

Effect of Growth Temperature during the Atomic Layer Deposition of the SrTiO₃ Seed Layer on the Properties of RuO₂/SrTiO₃/Ru Capacitors for Dynamic Random Access Memory Applications

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Figure S1. Surface morphologies of the as-deposited 4.5 nm STO seed layer grown at (a), (b) HT (370 °C) and (c), (d) LT (230 °C). (a) and (c) are the SEM images, and (b) and (d) are the AFM images.



Figure S2. The variations of the leakage current density of 10 nm STO films with LT (230 °C) and HT (370 °C) seed processes as a function of applied voltage. The bias was applied to the top electrode while the bottom electrode was grounded.



Figure S3. The ToF-SIMS depth profiles of (a) the 13-nm-thick TiO_2 grown at HT (370 °C) and (b) the 12-nm-thick TiO2 grown at LT (230 °C) on Ru substrates. (c) Comparison of the ToF-SIMS depth profiles of the C element in (a) and (b) in a linear Y-axis scale. The X-axis was normalized to match the thickness of two samples from the small thickness difference. HT TiO₂ were deposited for 200 cycles (50 minutes), and LT TiO₂ were deposited for 400 cycles (166 minutes) to match the thicknesses of the two films.