Supporting Information

Electrical-driven Plasmon Source on Silicon based on Quantum Tunneling

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1. Fowler-Nordheim tunneling of MIS (Metal-Insulator-Silicon) Tunnel Junction

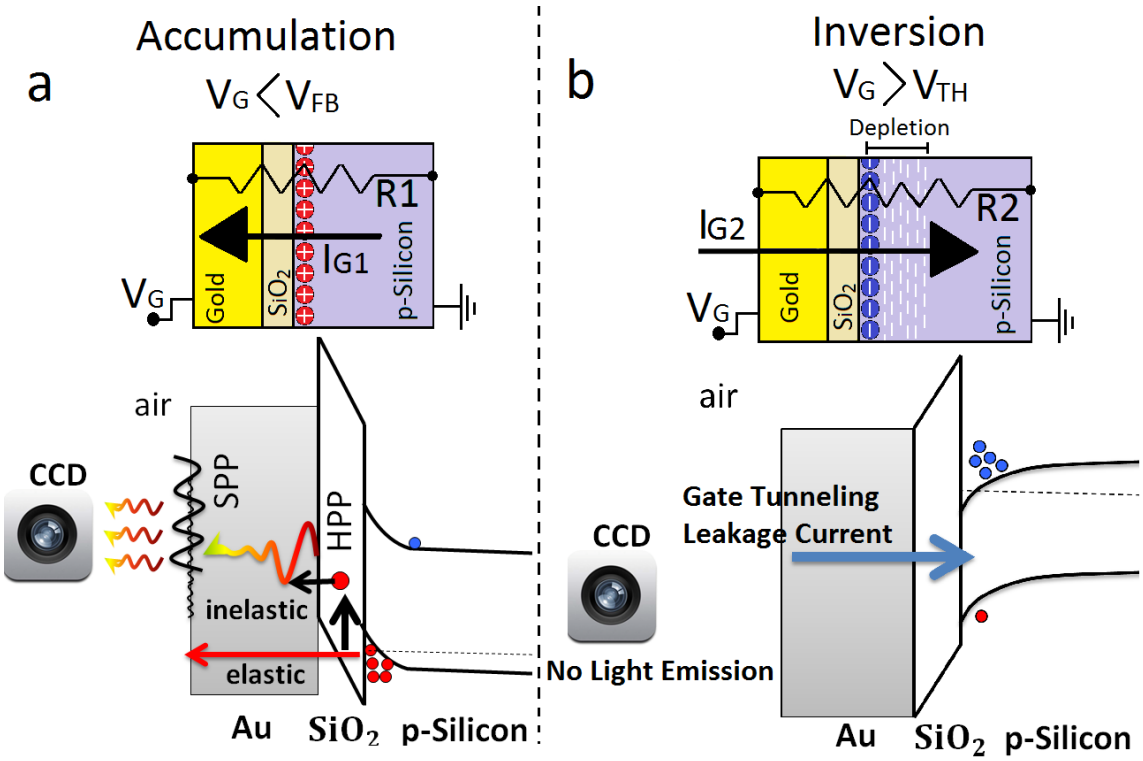

Figure S1. Energy diagram of p-type Si/SiO_2/Au tunnel junction **a,** when $V_{bias} < 0$ (Accumulation Region), **b,** when $V_{bias} > 0$ (Inversion Region)

The plasmon source from the main text relies on currents originating from a quantum tunnel events. The electrical and optical (plasmonic) interplay between current, voltage, and optical mode governs the performance of this device. The core is a metal-insulator-semiconductor structure based on a p-type Silicon-on-insulator substrate. While in a DC capacitor only charge-loading currents can low, here a thin oxide layer facilitates tunnel currents of holes from the semiconductor into the metal in accumulation (Fig. S1a). The current flow in accumulation consists of elastic and inelastic

tunneling (~7x10^{-3} A). On the other hand, the resistance between metal and silicon is rather high when in inversion, where only gate tunneling leakage current is occurs (around 1×10^{-12} A, Fig. S1b). Hence we can treat this tunnel source as an NMOS transistor and allow the creation of n-type channel between drain and source. The tunnel current density responsible from the plasmon emission is given in [1] and is proportional to the electric field in the oxide layer;

$$I \; \alpha \; {E_i}^2 \exp\left[-\frac{4\sqrt{2m^*}(q\phi_B)^{3/2}}{3q\hbar E_i}\right] \qquad (1)$$

where E_i is the electric field in the oxide region, m^* is an effective mas, ħ is plank constant, and ϕ_B is barrier height. The electric field in the insulator region is proportional to the surface potential and given in [2] as;

$$E_{ox}= \left(V_{bias} + \phi_{Bs} - \phi_{Bm} + \frac{k_B T}{e} ln\left(\frac{N_C}{N_D}\right) - \psi_s\right)/t_{ox} \qquad (2)$$

where V_{bias} is the applied bias voltage, ϕ_{Bs} is the difference between the electron affinities of Si and SiO_2, ϕ_{Bm} is the difference between the electron affinity of SiO_2 and the work function of the metal, t_{ox} is the oxide thickness and ψ_s is the surface potential. Both an increase in the tunneling current (1) or an increase in the applied bias voltage (2) result in a higher electric field in the insulator region (Fig. S2). Up to certain point, the tunneling current is ignorable and very small, however it shows a threshold effect in the IV curve when the electric field is high. This is accompanied by an increase in the light emission intensity.

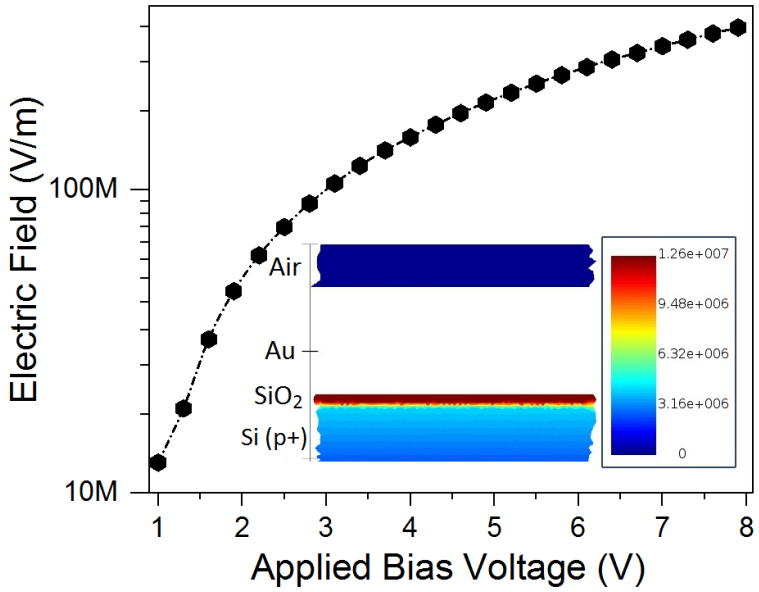

Figure S2. Lumerical Device Simulation for Electric Field Distribution at different applied bias voltage on a p-type Si (2µm) / SiO_2 (2.5 nm) /Au (20 nm) tunnel junction

In contrast to the case given in Fig. S1, it is possible to obtain light emission in both bias polarities (accumulation and inversion). It was achieved by simply introducing n+ doping to the p-Silicon. However, the magnitude of light emission is higher in inversion-compared accumulation although the magnitude of tunneling current in accumulation is higher [2]. This can be attributed to higher electric field at inversion, which results in a higher tunneling rate comprised of hot-electrons, thus feeding the surface plasmon polariton (SPP) mode and the top metal-air interface of the device, resulting in a higher observed light emission.

2. Numerical Simulation of Light Emitting Metal-Insulator-Silicon Tunnel Junctions

Two different numerical programs (Lumerical FDTD and Wavenology FDTD) were used to simulate the MIS structure in this work. In one case, bias voltage was used to create the emission and in the other case, dipoles were located in oxide layer to imitate the emission.

For the model built in Wavenology FDTD: Silicon substrate, SiO_2 and Au films are taken to be 2 μm, 2 nm and 100 nm thick, respectively. The dispersive permittivity of Si and SiO_2 are taken from [3], whereas complex permittivity of Au is taken from [4]. As shown in Fig. S3, a 250 nm x 1 μm region is assumed to be etched 1.5 μm far from the plate where voltage is applied. In order to prevent any plasmonic effects, which might come from the plate, the plate itself is assumed to be a perfect-electrical conductor (PEC). Another very thin PEC film placed under the Si substrate and a DC voltage is applied between these two PEC spots. Wavenology solves for circuit and Maxwell's equations simultaneously on the same grid using finite-difference time-domain (FDTD) method. To guarantee high numerical accuracy, a 30 points-per-wavelength sampling density is utilized over the whole simulation domain. In order to take doping level into account, the conductivity of Si is set to $\sigma = q(\mu_n n + \mu_p p)$, where μ_n and μ_p are the mobility of electrons and holes, respectively; where n and p are their doping levels.

For the model built in Lumerical FDTD: Dipoles are located in oxide layer to imitate the light emission while a surface roughness on 20nm thick Gold (index from Palik) layer is created in MIS structure. A high mesh FDTD (8/8) with a stability factor of 0.95 was applied. An extra high mesh box was added to get further improvement in accuracy. Both Lumerical FDTD and Wavenology FDTD show a double-peak spectrum that match the measurement centered around 720 nm and 550 nm (Fig. S4a). The overall shape is not simply given by the quantum condition $E = h\nu = qV_{bias}$, but depends on the convolution of the spectrally dispersive tunnel current density with that of the eigenmode of the system, namely the hybrid photon plasmon mode [5]. The spectral power density depends on current-fluctuations leading to plasmon creation; small fluctuations in the tunnel current lead to electric field fluctuations, which in turn accelerate and decelerated electrical carriers acting as a plasmon source. As such the spectral dispersion of the internal hybrid plasmon mode is material sensitive [5]. Following this line of thought, our modeling confirms the experimentally observed spectral double peak with exponential decaying emission intensity (Fig. S4a) [5, 6].

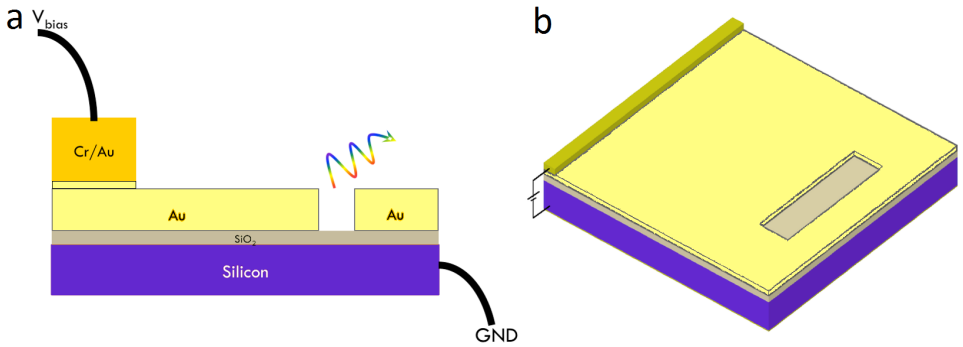

Figure S3. a, Two-dimensional and **b,** three-dimensional view of the simulated structure in Wavenology

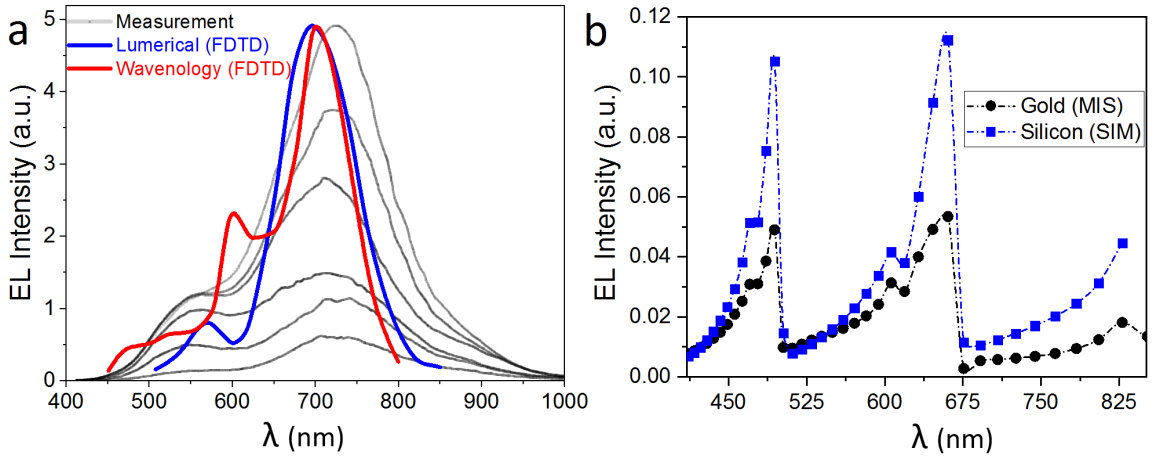

Figure S4. a, The junction's spectrum is centered around 720 nm increases with bias in steps of one Volt. Lumerical FDTD simulation result for 20 nm thick Gold (with surface roughness), when dipoles are used as a light emission source and Wavenology FDTD results for 20nm thick Gold when Voltage source is applied to create emission. **b,** Emission performance comparison between MIS and SIM structures in Lumerical FDTD

Further studies were conducted via building the SIM (Silicon-insulator-metal) to compare its emission performance with MIS (metal-insulator-silicon) (Fig. S4b). Results show a higher emission intensity for the SIM structure simply because of the lower absorption of the semiconductor than the metal.

3. Grating Design, Experimental Test, and Analysis

Technologically a higher light output is desired for a light source. Since the top metal blocks the emission normal to the sample via absorption, flipping the metal insulator semiconductor (MIS) tunnel junction up-side-down to an SIM configuration (i.e. metal at bottom, and semiconductor on top) renders the use of established silicon-on-insulator (SOI) platforms unusable. Hence our design and approach is based on an SOI MIS configuration. Here, light emission is still limited by the top metal, which can be reduced, however by thinning the top metal. A second option to obtain higher light output is trivial and would be to increase the bias voltage. However thermal non-linearity leads to instabilities of the device, whereas the electric field breakdown voltage sets a fundamental upper voltage limit. Optically, the device operation involves three optical modes, which we discuss next from the inside out; (i) a hybrid plasmon polariton mode inside the MIS tunnel junction termed HPP mode, (ii) a SPP mode at the top of the metal-air interface, and (iii) free space photons leaving the device and being captured by the naked eye/detector/camera. In operation both the HPP- and SPP modes are intrinsically nonradiative. Increasing the overall outcoupling efficiency requires a facilitating improved coupling between all three involved modes [7] via wavevector matching, which can be achieved either by dispersion engineering, or via a grating structure [8]. There are a variety of parameters effecting the MIS diode's light emission intensity (I_e) with respect to grating parameters (Λ, d, Θ, and ϵ) [5, 7-14];

$$I_e \approx \frac{P(k,w)}{exp\left(\frac{\lambda_e}{L_x}\right)} \quad where\ L_x = \frac{1}{2k_i}, k = Ksin\Theta \pm nG,\ G = \frac{2\pi}{\Lambda},\ \ k, k_i \sim \frac{\epsilon}{t_{ox}} \qquad (1)$$

where □ is the corresponding wavelength, k is the momentum, n = 1,2,3…, Θ is the emission angle, λ_e is the effective wavelength, Λ is the grating period, t_{ox} and ϵ are the thickness and dielectric constant of oxide layer respectively. Increase in the light emission intensity (I_e) with respect to

increase in Θ and ϵ or decrease in t_{ox} and Λ are expected due to increase in k and decrease in L_x (1) as demonstrated in [9] and [5]. Furthermore, coupling the HPP mode efficiently into the light requires $\Lambda \sim \lambda_e$ where $\lambda_e < 80\ nm$ (3 eV) [5]. However, the gratings duty cycle also affects the light emission efficiency (Fig. S5). We investigated the grating impact via a grating shape-dependent analysis. Here we assumed the metal thickness optimized (20 nm) case; the grating angle was kept constant as it only depends on the beam diameter of the focused-ion-beam (FIB) in the fabrication process, while the duty cycle was changed to create different grating shapes. The advantage of this approach (changing duty cycle) is basically to eliminate the necessity of using tiny grating period ($\Lambda \sim \lambda_e$ where $\lambda_e < 80$ nm (3 eV) [5]), which may be challenging for during FIB ion milling, which could also lead to challenges in production yield for actual technology. The Lumerical simulation results with different duty cycle and its spectrum (Fig. S5) suggests that there is an optimum duty cycle (a = 25 nm) with respect to obtaining maximum light emission intensity.

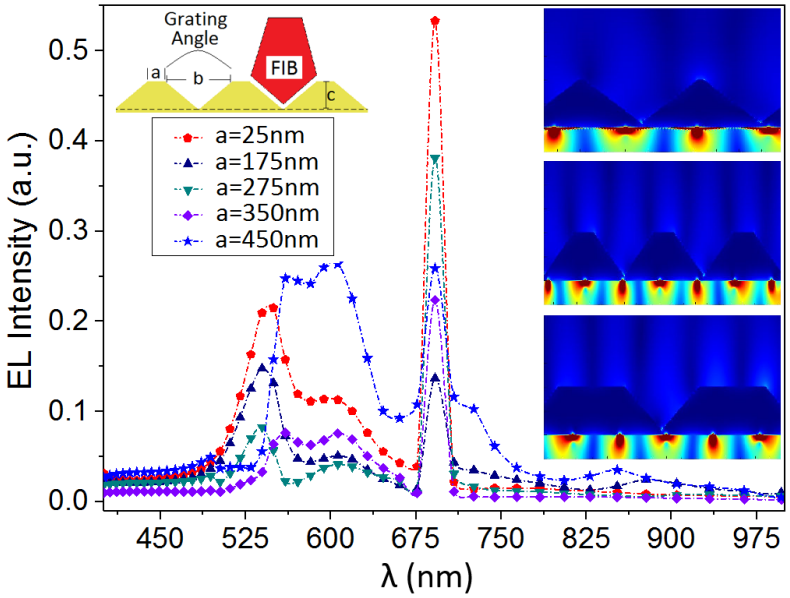

Figure S5. The spectrum and light emission profile for different duty cycle derived by Lumerical simulation, where a represents duty cycle and c represents the grating thickness.

4. Emission Efficiency and Relative Efficiency

The external, or wall-plug, quantum efficiency ($\eta_{wallplug}$) of the light emitting tunnel junction's emission is given by the product of two factors; namely the internal light (here plasmon) creation (η_{int}) times an outcoupling efficiency factor, simply via:

$$\eta_{wallplug} = \eta_{\text{int}} \cdot \eta_{outcouple} \quad (1)$$

Our procedure to obtain a numerical value for Eqn (1) is as follows; (i) we measure the captured optical power from the emitting device using a CCD camera by integrating over the number of pixels times their grey-scale level, thus obtaining a single scalar representative of the optical power captured by the camera. (ii) Calibrate the optical power captured by an LED with similar spectral response to the tunnel junction, and again obtain an integrated scalar. (iii) Dividing the two values from (i) and (ii), we obtain a value for $\eta_{wallplug}$, which we found to be $4.8(\pm 3.5)\times 10^{-4}$. We note, however, that this value varies depending on the history on the sample, applied bias, and device

junction size. For instance, we find that the conversion efficiency initially increases with bias to about 4-5V, and then sharply drops. In addition, we find that smaller junctions show higher conversion efficiency than large ones (details reported elsewhere). Both effects suggest resistive, and likely thermo-resistive effects inside the junction where high device temperatures increase the resistance due to joule heating.

All devices were operated a room temperature and non-thermo-stabilized to probe the intrinsic behavior of the devices. To control performance, actual devices should be thermally stabilized, and/or cooled. The decline in the conversion efficiency with bias is also evident as each device could be driven to failure where metal oxidation occurred, accompanied by oxide break-down, and a dramatic reduction in photon emission (low conversion despite a near-shorted device). This effect is observed in Fig. 3e of the main text. In addition, cycling this light source for actual large-signal modulation (see supplementary video) stresses the oxide by introducing defect states. This lowers the effective oxide over time and reduces the conversion efficiency.

In order to gain further insights into the two components on the right-hand-side of (1), we performance numerical simulations to estimate the outcoupling efficiency to free space facilitated by the grating. The numerical simulations (Fig. 3f main text) suggest an outcoupling enhancement factor of about 4-fold. To confirm this, we treat this as an antenna problem by taking the ratio of an estimated source impedance ($R_{radiation}$) of the plasmon MIS mode without grating and the free-space impedance (z_0 = 377Ω). Thus, averaging the effect of the grating (8x + 3x)/2 ~ 5x improvement which matches our observed 4x well. The effective wavelength (λ_{MIS}) in Eqn (2) depends on which method is used to determine the optical modal area [15]. The parameter a is the physical length of the radiating antenna, and here approximated by a radiating dipole equivalent to the size of the effective mode wavelength.

$$R_{radiation} = \frac{\omega^2}{6\pi\varepsilon_0 c^3}\cdot a^2 = \sqrt{\frac{\mu_0}{\varepsilon_0}}\frac{2\pi}{3}\left(\frac{a}{\lambda}\right)^2$$

$$with$$

$$a \propto \lambda_{MIS} \cong \lambda_0 \cdot \left[\frac{1}{4},\frac{1}{3}\right] \quad and \quad z_0 = \sqrt{\frac{\mu_0}{\varepsilon_0}} = 377\Omega \qquad (2)$$

$$\eta_{outcouple} \approx \frac{R_{radiation}}{z_0} = \left[12.5,33.3\%\right]$$

With results from (2) we can estimate the internal quantum efficiency, η_{int}, to be $O \sim 10^{-4}$. Naturally, an engineering aim would be to increase this conversion efficiency. Here, we note that the Purcell effect, which helps to accelerate the downward transition of an excited state and thus facilitates increasing the brightness of an emitter, cannot be used to enhance η_{int}. This is because the temporal response of the tunnel process is on the order of a femtosecond (using Heisenberg's uncertainty principle, and $\lambda_{emission} \sim 2eV$).

The outcoupling efficiency is calculated as 5x (2), and derived as 4x via Lumerical FDTD. These two findings are reasonably close to the ratio of 3.1x (between sine shape grating and no-grating) at 8V (Main Manuscript Figure 3e) where the increase in efficiency are maximized and saturated for all three devices. All three devices are very close to failure due to joule heating and relatively high thermal stress (Fig S6). That is why, the outcoupling efficiency can be estimated to be 4x. The

relative efficiency increases up to 40.9x at 5.1 V (Figure 3e main manuscript), where the outcoupling efficiency is assumed to be 4x. That's why the increase in the internal efficiency is derived as 10x (40.9/4=10).

5. Device Reliability

Metal (20 nm Au)-insulator (2.5 nm SiO_2)-Silicon (500 µm) structure was built in Coventor to study the thermal stress. Applying DC bias voltage between top metal and substrate (silicon) results in joule heating and can cause device failure due to high thermal stresses. The electrical conductance is derived from measurement for each applied bias voltage and imported into Coventor simulation. The current density in simulation match our experimental measurements well (Fig. S6). The temperature profile and thermal stress originating from Joule heating were derived from Coventor simulation for each applied bias voltage (Fig. S6c). The temperature on substrate (Silicon) bottom is assumed to be 300 K (Room temperature). A high mesh density was used for more accurate results. The maximum stress was found as 150 MPa when 8 V bias voltage applied on the device. This is close but still below an ultimate strength of any material used in device fabrication. In another words, any small further increase in voltage bias beyond this point may result in device failure [16]. Indeed, most experimental devices biased beyond 8V shorted. On the other hand, the thermal stress at 5.3 V is around 45 MPa, which is well below the ultimate tensile strength of each material in the junction. This demonstrates that the LETJ device in this work should be robust and reliable at 5.3 V. However, between 6-8 Volts we do observe a decline in the electroluminescence-voltage output, which we contribute to excessive heating.

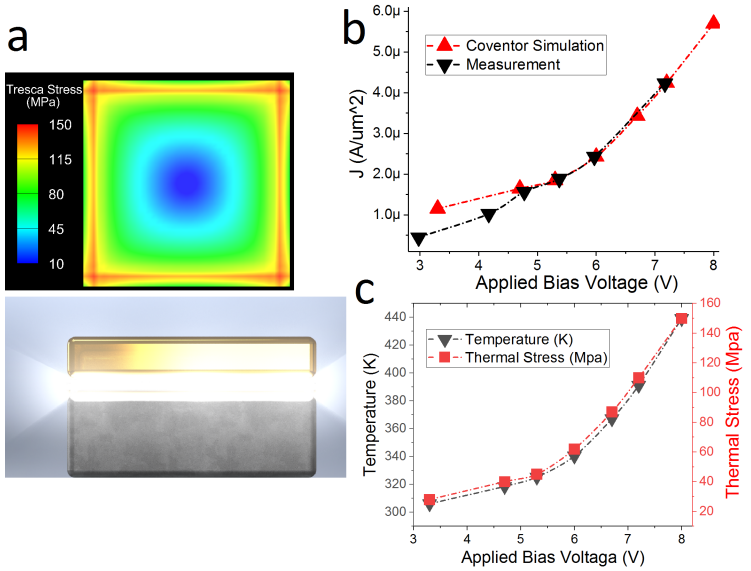

Figure S6. a, Thermal stress profile on oxide-metal interface cross section from top view for Au (20 nm) / SiO_2 (2.5 nm) / Si (500 µm) at 8V **b,** Current density versus applied bias voltage **c,** Thermal stress and temperature with respect to applied bias voltage

6. Cut off Frequency Prediction

Because the emission originates from the rapidly-thermalized Fermi-sea of a semiconductor and into the conduction band of a metal, the limiting processes do not follow the standard rate equations of light emitters and lasers. From Heisenberg's uncertainty principle, large optical bandwidths imply inelastic tunneling speeds on the order of 10's of femtoseconds. Indeed, the temporal response of a tunnel event has been measured as short as 100 atto seconds [17]. Comparing this to recombination lifetimes of direct and indirect bandgap semiconductors such as GaAs and Si, which

are on the order of nanoseconds and milliseconds, respectively, we find that tunnel junctions may allow for a high modulation speed [13, 18]. With the delay of the actual tunnel being negligible, we analyze the electrical circuit-related constrains to understand the junction's actual response time. The limiting factor is related to resistive and capacitive (RC) effects of the junction itself [19]. Our MIS tunnel source is a planar structure acting as a parallel plate capacitor (Fig. S7). Here, the relevant resistance in this case is not the line impedance but the resistance. For inelastic tunneling events to be dominant, the electron tunnel current must dominate the displacement current across the capacitor. Note, that the tunnel resistance scales inversely with area, whereas capacitance scales linearly, yielding an RC time constant invariant to area in an ideal case. However, the tunnel resistance scales exponentially with thickness, while the capacitance scales only linearly. As a result, high modulation speed (>40 GHz) can be achieved with sufficiently thin tunnel oxides (0.6 nm, Fig. S7). The latter is technologically achievable by adjusting the deposition cycle in the atomic-layer-deposition process (Fig. S7) [20, 21]. The equivalent circuit of the MIS diode was derived as parallel RC [22] and the cut off frequency of RC is;

$$f_c = \frac{1}{2\pi RC}, \qquad \mathrm{R} = \frac{V_{bias}}{JA}, \qquad \mathrm{C} = \epsilon_0 \epsilon_r \frac{\mathrm{A}}{t_{ox}}$$

where J is the tunneling current density and was derived using Silvaco where the Silicon thickness is 200 nm for both PIS and MIS device. Replacing the top metal of the MIS junction with a poly-silicon drops the speed to ~8 GHz due to lower tunneling current originating from the higher resistance of the doped semiconductor vs. the metal (Fig. S7).

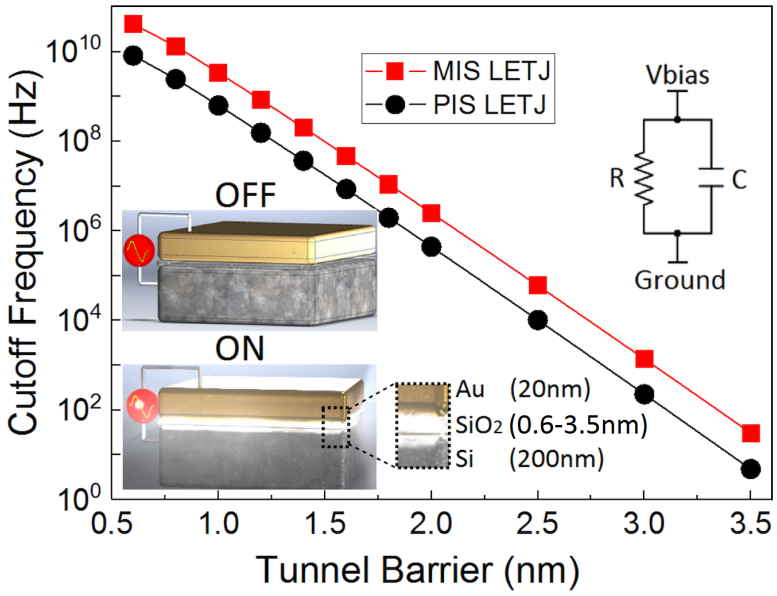

Figure S7. Direct modulation speed of the tunnel junction. Results show that at 10's of GHz-fast modulation are possible for tunnel oxides less than one nanometer (V_{bias} = -3.4V). MIS = metal-insulator-semiconductor and PIS = polysilicon-insulator-semiconductor. Silicon thickness = 200 nm Inset: plasmon emitting tunnel junction layout and its equivalent circuit model.

It is worth mentioning, that the metal serves a triple function in this light source; (i) metal confines the optical mode enabling device scalability via allowing for sub-diffraction limited modes as we have previously shown for hybrid plasmons [23], (ii) metal is a heat sync, since replacing the top metal with poly Silicon lowers the device temperature enabling higher modulation speeds (i.e. $P_{dissipated} = E/bit$ x $bitrate$) [23], and (iii) metal acts as an electrical contact allowing for low-voltage drops in the contacts leading up to the device. The latter is not possible for photonic devices as their optical loss from heavy-doped (low resistance) semiconductors is detrimental to the insertion loss

devices [24]. Interestingly, the modulation speed can be accelerated further by increasing the inelastic tunneling probability via the Purcell factor, which could be achieved by introducing nanoscale cavities [25-27]. Such acceleration of emission processes will thus further decrease the tunneling resistance, hence increasing direct modulation speed. This also leads to an enhanced quantum efficiency and thus wall-plug efficiency, in analogy to the spontaneous emission factor reducing the laser threshold [28].

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