Supporting Information for "Electrically Tunable, CMOS-Compatible Metamaterial Based on Semiconductor Nanopillars"

Matthew Morea[*,†], *Kai Zang*[†,§], *Theodore I. Kamins*[†], *Mark L. Brongersma*[‡], *and James S. Harris*[†]

[†]Department of Electrical Engineering and [‡]Geballe Laboratory for Advanced Materials, Stanford University, Stanford, California 94305, United States

Present Address: § Microsoft Corporation, 1 Microsoft Way, Redmond, WA 98052

*Corresponding Author: mmorea@stanford.edu

1. Other Fabrication Details and SEM Images

During fabrication, two sets of devices were attempted with different etch depth for the nanopillars (Figure S1). Ge nanopillars of height around 500 nm and 700 nm (Figures S1a and S1b) were successfully made. However, during subsequent processing, the taller pillars collapsed and suffered from stiction problems likely from the surface tension forces of liquid-based cleaning procedures or from photoresist coating (Figures S1d and S1f). The 500-nm-tall nanopillars were much less fragile (Figures S1c and S1e). Even taller nanopillars could be etched, and, by adopting fabrication techniques used for Micro-Electro-Mechanical Systems (MEMS) such as critical-point drying or hydrofluoric acid (HF) vapor, one may be able to create complete capacitor devices with them.

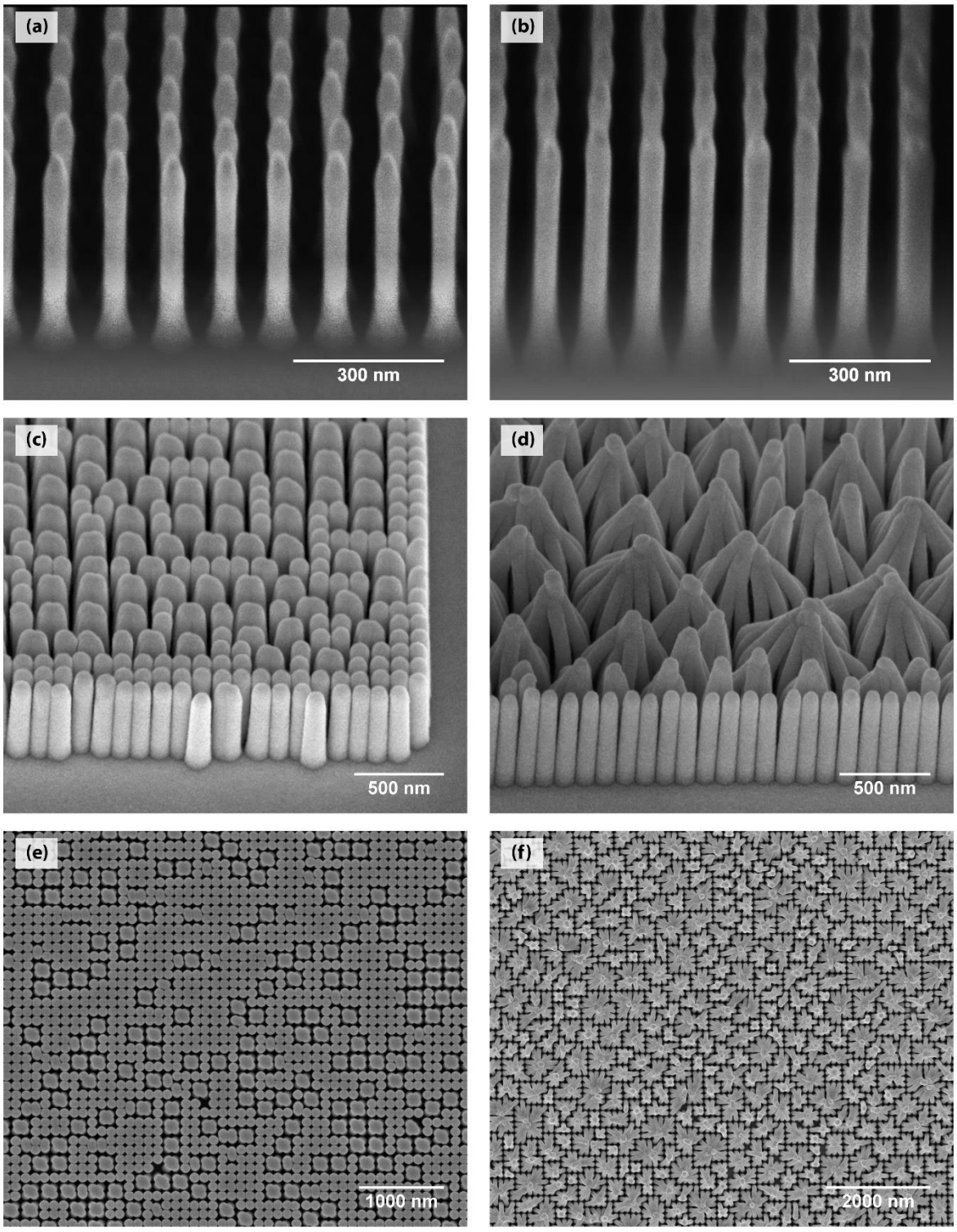

Figure S1. SEM images of nanopillars with height of (a, c, e) 500 nm and (b, d, f) 700 nm. (a/b) Images taken at 45° tilt of Ge nanopillars right after etching (without gate oxides and AZO). (c-f) Finalized devices (after metallization step) with gate oxides and AZO deposited on the nanopillars at different tilts: (c/d) at 45° tilt and (e/f) at 0° tilt. The taller nanopillars are more fragile and collapse from wet processing and spin coating steps (d/f) after the initial dry etch step (b).

2. Electrical Characterization

As noted in the main manuscript, the capacitance of our devices is improved with the use of nanopillars compared to planar devices. This enhancement corresponds directly with the increase in surface area due to the conformal coating of gate oxides and AZO around the Ge nanopillars. Even with such large surface area and non-planar surface, the gate oxide provides excellent isolation by keeping the leakage current low, specifically within the picoampere range (< 200 pA) between -2 V and 2 V for capacitors with diameter of 200 μm.

The devices are also capable of high-frequency operation (Figure S2), limited mostly by the RC time constant due to the large size of the tested capacitors. If such devices were arranged as pixels in a phased array, the devices could work at MHz or even GHz speeds because the area of each capacitor would be much smaller, leading to lower series resistance in the AZO and lower capacitance. Such speeds would be more than adequate for beam steering and many other applications.

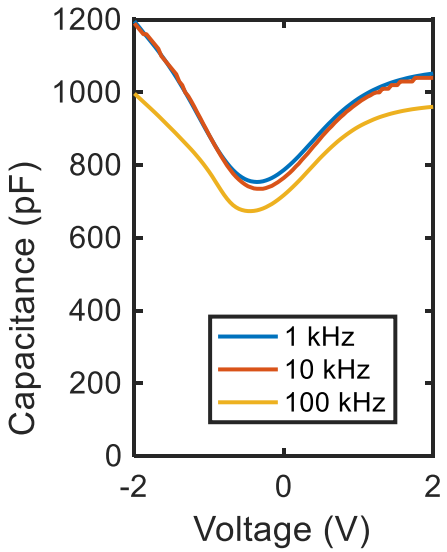

Figure S2. C-V measurement of a capacitor with nanopillars at frequencies from 1 kHz to 100 kHz (with diameter of 200 μm). At 100 kHz, the measured capacitance values start to decrease.

3. More Optical Measurement Results

Since our electron-beam lithography step uses an exposure dose array, we obtain nanopillars of varying diameter for each of the capacitor devices for every die. Individual dies are processed separately for PMMA development, metal mask deposition and lift-off, and dry etching of Ge

nanopillars; thus, the exact range of diameters may change for each die. The total range of diameters for the Ge nanopillars across multiple dies is about 20 to 50 nm. Looking at the FTIR reflectance for these different diameters as well as the devices without nanopillars (Figure S3), we can better understand some of the resonances in the spectra. For increasing diameter, the resonances appear to redshift moderately. Similar resonances can be observed in the planar devices, which are attributed to the Fabry–Pérot interference of the different layers of the material stack. Also, for devices with nanopillars, the reflectance is greatly reduced at lower wavelengths (i.e., 1 to 5 µm) compared to the planar devices, because the use of nanopillars increases the amount of interaction of light with AZO and, hence, increases loss. Tuning the nanopillar diameter is one way to get closer to the critical coupling condition (where reflectance approaches 0%), which would allow for large phase modulation.

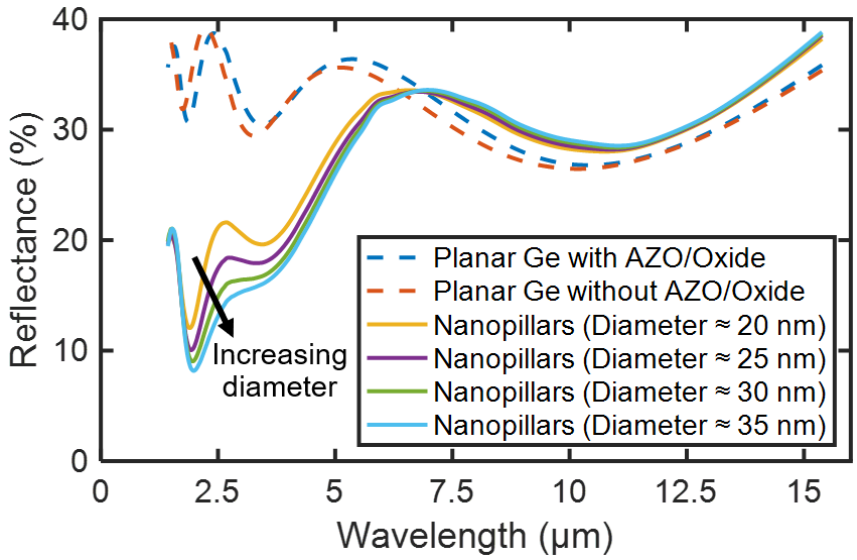

Figure S3. Unmodulated FTIR reflectance measurements for devices with varying diameter as well as those without nanopillars. The nanopillars are coated with the gate oxide and AZO layers. For this particular die, the diameters ranged from about 20 nm to 35 nm (i.e., the Ge pillar diameter, not including the added thickness from the outer coating layers). Increasing the diameter of the nanopillars redshifts the resonances. Also, similar Fabry–Pérot resonances can be observed in the planar devices.

Another way to characterize the modulation of the optical spectra with voltage is differential reflectance (Figure S4). For our device, the differential reflectance could be up to 40% when comparing the spectra at -4 V and at 4 V for the sharp resonance near 2.5 µm.

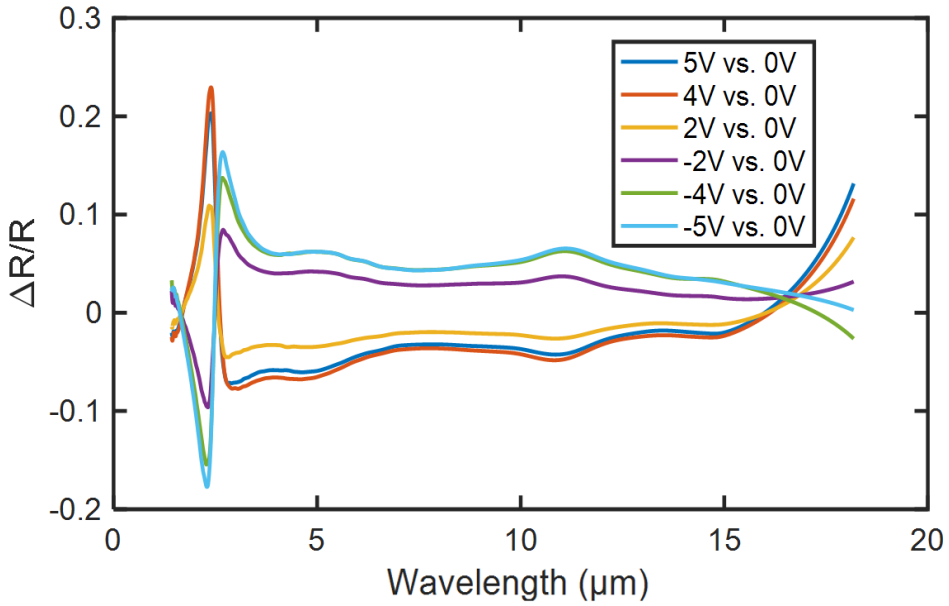

Figure S4. Differential reflectance at different bias voltages compared to the unbiased state of 0 V, calculated from measurement results shown in Figure 3 of the main text. At a wavelength near 2.5 μm, there is up to 20% differential reflectance for ±5 V vs. 0 V or up to 40% for -5 V to 5 V.

4. TMM Metamaterial Simulations

Another important parameter to consider when optimizing phase modulation is the Ge film thickness underneath the metamaterial layer (i.e., the nanopillar array). This film provides a Fabry-Pérot resonance that enhances the light interaction with the metamaterial layer; hence, the phase modulation has a periodic behavior as a function of the film thickness (Figure S5).

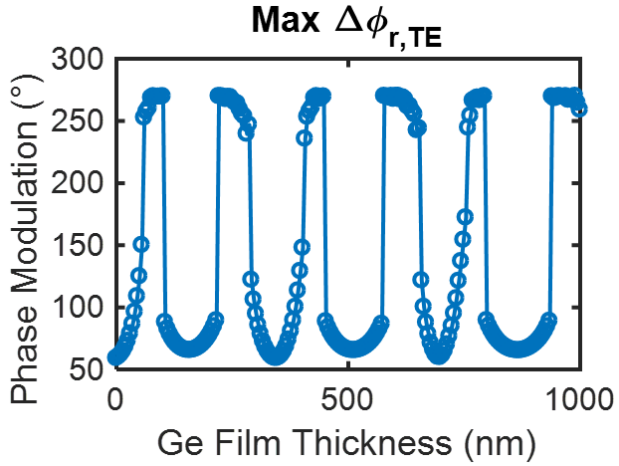

Figure S5. Phase modulation as a function of the Ge film thickness underneath the nanopillar array. Simulated with pillar height of 500 nm, diameter of 40 nm, and incident angle of 35°.

5. Device Physics and FDTD Simulations

Full device physics and optical simulations of our nanopillar capacitor structures were done using Synopsys Sentaurus and Lumerical FDTD Solutions. With a quantum mechanical description of carriers in our SOS capacitor, we can see that the accumulation region extends only a few nanometers into the Ge or AZO materials (Figure 2c); thus, to improve the electrical modulation, we chose to study tightly packed nanopillars to increase the effective surface area. Using the carrier distributions from Sentaurus, we can create a distribution of optical permittivity values based on the Drude model for AZO and Ge within a 3D nanopillar for positive, negative, and zero voltages. For the devices fabricated with 430-nm-tall nanopillars, we can see close agreement between our FDTD simulations and the measured reflectance from FTIR (Figure S6).

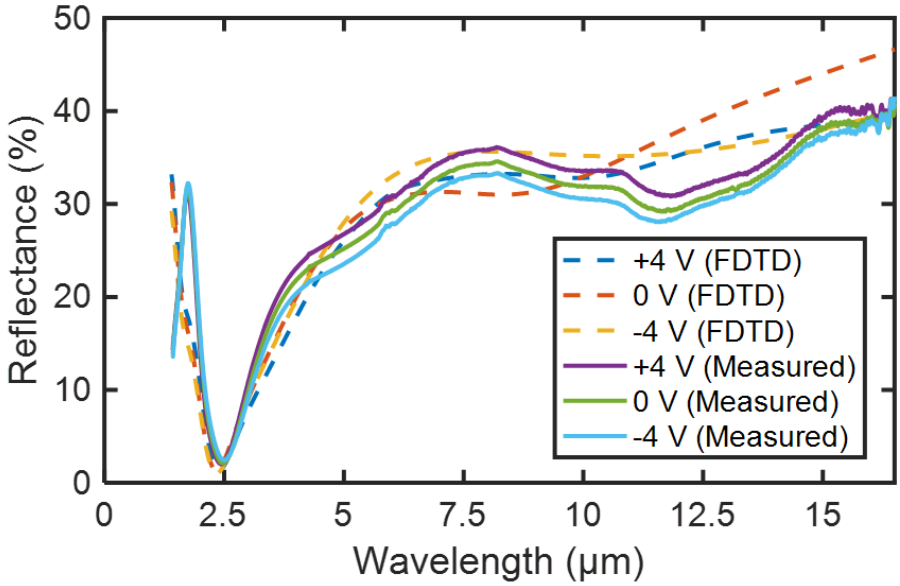

Figure S6. FDTD simulation of reflection with unpolarized light incident at 35°, compared with measured FTIR reflectance for nanopillars with height of 430 nm.

6. Transmission and Absorption

Near critical coupling, the reflectance is minimized; however, the device is not a perfect absorber due to the transparency of the Si substrate for wavelengths above 1.1 μm (Figure S7). Also, as noted in the main text, the use of a back reflector with a thinner substrate could possibly improve the optical efficiency for phase modulation, because more light would interact with the tunable metamaterial layer.

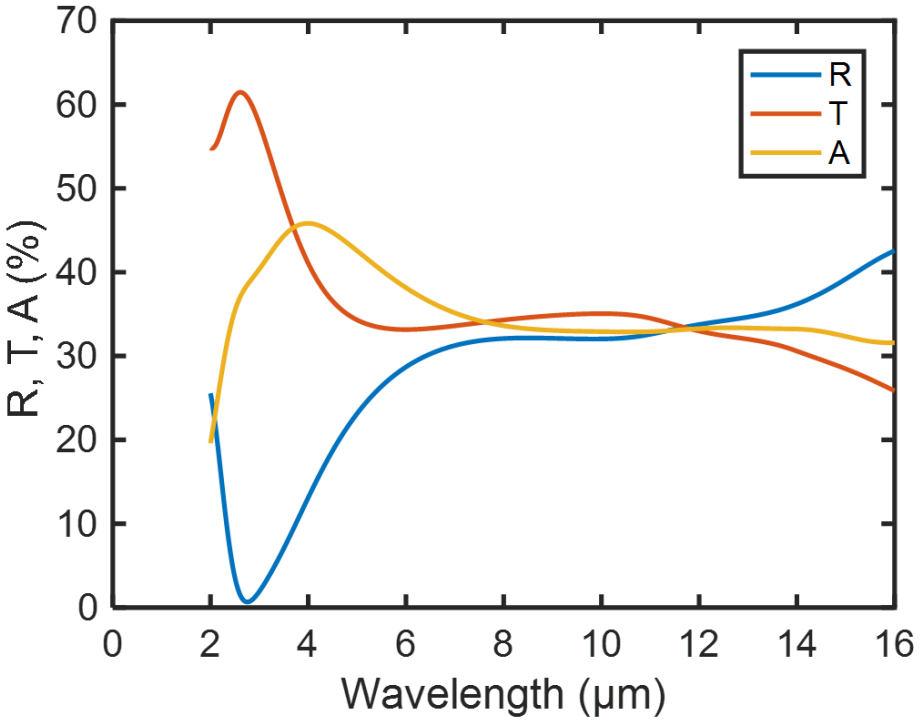

Figure S7. TMM simulation of reflection, transmission, and absorption for metamaterial-Ge-Si stack as described in Figure 5a-b in the main text. At the wavelength of minimum reflectance, the transmission is close to 50%; thus, the device is not a perfect absorber at this point.