Supporting Information

Visible light-erasable oxide FET-based non-volatile memory operated with deep trap interface

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PEALD and in-situ H_2-plasma treatment

Figure S1 shows the pulse sequence of the PEALD used to deposit the Al_2O_3 and TiO_2 films.[1,2] The Al and Ti metal precursors were trimethyl aluminum (TMA) and titanium (IV) tetraisoproxide (TTIP), respectively, and O_2 plasma was used as the oxygen source. The reservoirs of TMA and TTIP were kept at 25 °C and 70 °C, respectively. Argon carrier gas was supplied with a flow rate of 100 sccm. The Al_2O_3 and TiO_2 films were deposited at a temperature and RF power of 300 °C and 150 W, respectively. The growth rates of Al_2O_3 and TiO_2 were 1.11 Å per cycle and 0.46 Å per cycle, respectively. For the in-situ H_2-plasma treatment, hydrogen was supplied with a flow rate of 200 sccm, and the same temperature and RF power were used.

Surface roughness of Al_2O_3 and TiO_2 films measured using AFM

Figure S2 (a) and (b) show the 2D and 3D AFM images, respectively, of an 80 nm Al_2O_3 thin film deposited by PEALD at 300 °C on a Si substrate. The average surface roughness was 0.21 nm, indicating that the Al_2O_3 thin film had a very flat surface, even at a thickness of 80 nm. Figure S2 (c) and (d) show AFM images of a 30 nm TiO_2 thin film deposited by PEALD at 300 °C on the Al_2O_3 film. The surface roughness value increased to 1.68 nm after TiO_2 deposition. This means that the 30 nm TiO_2 was crystallized (anatase phase) on the Al_2O_3 film during deposition at 300 °C.

Characterization of the electrical properties of the TOFDI TiO_2 flash memory devices.

The threshold voltage (V_{th}) of 0.5 V was calculated from the slope of the square root of the drain current ($I_D^{1/2}$) vs. V_G curve shown in Figure 4 (c). The field-effect mobility (μ_{FE}) for the device with a channel length/width (L/W) = 10 μm/40 μm, as shown in Figure 4 (c), was 1.2 $cm^2V^{-1}s^{-1}$,

superior to the values previously reported for TiO_2 MOSFETs (μ_{FE}: 0.672 $cm^2V^{-1}s^{-1}$) fabricated using ALD.[3] The μ_{FE} was determined using the following equation[4]:

$$\mu_{FE} = \frac{Lg_m}{WC_{ox}V_D} \quad (1)$$

where, g_m and C_{ox} are the transconductance (obtained from I_D vs. V_G curves) and the capacitance per unit area of the gate insulator, respectively.

Electrical characteristics of the devices fabricated with and without H_2 treatment

Figure S3 (a) and (b) show the hysteresis of the transfer curves for the devices prepared with and without H_2 treatment. From the forward (V_G = −20 to 30 V) and subsequent reverse sweeps (30 to −20 V), the samples with and without H_2 plasma treatment typically showed clockwise hysteresis. This indicates that the trapped mobile carriers were a dominant factor contributing to the hysteresis.[5] The magnitude of the threshold voltage shift (ΔV_{th}) for the sample without H_2 treatment was 9.5 V, while those for the H_2-treated samples at 12 s and 24 s were 5 V and 3 V, respectively, as shown in Table S1. The magnitude of ΔV_{th} did not decrease further as the treatment time increased to 36 s. This demonstrated that the hydrogen atoms effectively passivated the shallow trap sites.

Breakdown characteristic curve of Al_2O_3 and the gate current measured with the programming voltage

The breakdown characteristic curve of 80 nm-thick Al_2O_3 was measured, as shown in Figure S4(a). In the previous paper published in our group, the breakdown electric field of 30 nm-thick Al_2O_3 deposited using the same equipment as this experiment was 10 MV/cm.[6] Similarly, the breakdown electric field of 80 nm-thick Al_2O_3 was 10 MV/cm (Figure S4(a)). Also, we

measured the gate current with the programming voltage of 50 V (Figure S4(b)). This result shows that gate current (I_G) were 5-orders of magnitude lower than I_D.

Energy band diagrams and memory operations

To well understand the electrical program and VL erase mechanisms of the TOFDI TiO_2 memory, we added the energy band diagrams and memory operations. Figure S5(a) shows energy band diagrams and initial state in the TOFDI TiO_2 memory. Note that the shallow level trap and deep level trap at the interface are relative concepts. The trap levels above E_F is referred to as the shallow level and the one below E_F is referred to as the deep level.[7,8] In Figure S5(b), when a positive V_G pulse was applied for programming the memory, shallow and deep trap sites at the interface between TiO_2 and Al_2O_3 capture electrons in the channel. The trapped electrons recombine with holes photo-generated by the VL irradiation (Figure S5(c)) to form neutral trap sites, and the initial state can be fully recovered (Figure S5(a)).

Cycling tests of the TOFDI TiO_2 memory

The cycling tests for 100 times were performed, as shown in Figure S6. We cautiously claim that the cycling tests for 100 times show the stability of memory operation pretty well because the degradation of device characteristics usually occurs very early.

Supplementary Table and Figures

Table S1. Electrical properties of TOFDI TiO_2 flash memory devices prepared with or without H_2 treatment.

H_2 treatment time	μ_{FE} ($cm^2 V^{-1}s^{-1}$)	V_{th} (V)	On/off ratio	Hysteresis (ΔV_{th})
0 s	1.2 (σ = 0.09)	- 0.5 (σ = 1)	~ 10^7	9.0 (σ = 0.61)
12 s	1.5 (σ = 0.09)	- 2.0 (σ = 0.35)	~ 10^7	5.1 (σ = 0.55)
24 s	1.4 (σ = 0.04)	- 2.7 (σ = 0.42)	~ 10^7	3.1 (σ = 0.47)
36 s	1.4 (σ = 0.10)	- 3.1 (σ = 0.22)	~ 10^7	3.2 (σ = 0.21)

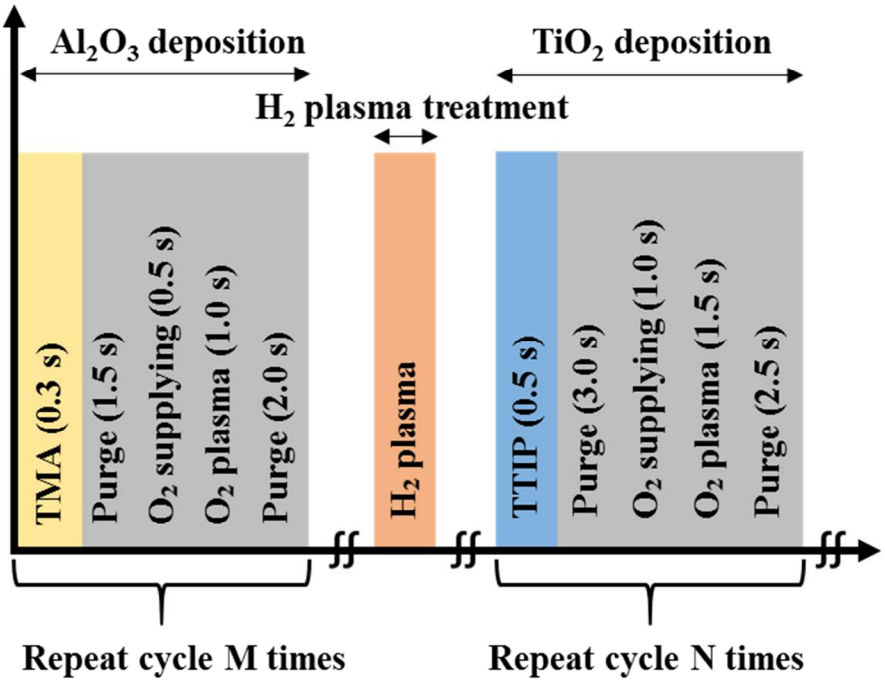

Figure S1. Schematic diagram showing the PEALD process and in-situ H_2 plasma treatment process for preparing the Al_2O_3 and TiO_2 films.

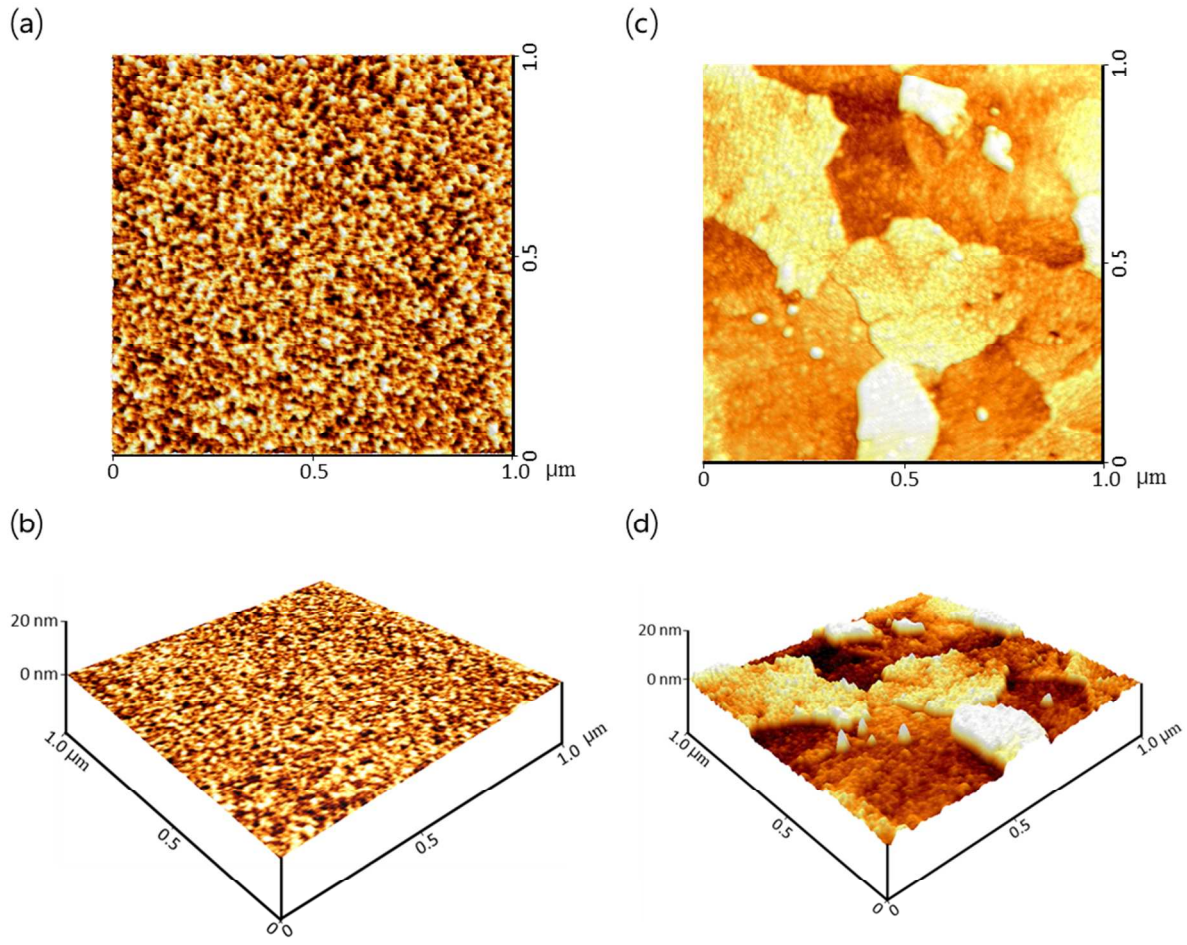

Figure S2. (a, c) 2D and b, d) 3D AFM micrographs (1 µm × 1 µm) for (a, b) Al_2O_3 thin films deposited on Si substrates and (c, d) TiO_2 thin films deposited onto the Al_2O_3 films. The root mean square (rms) surface roughness of the Al_2O_3 and TiO_2 films are 0.21 nm and 1.68 nm, respectively.

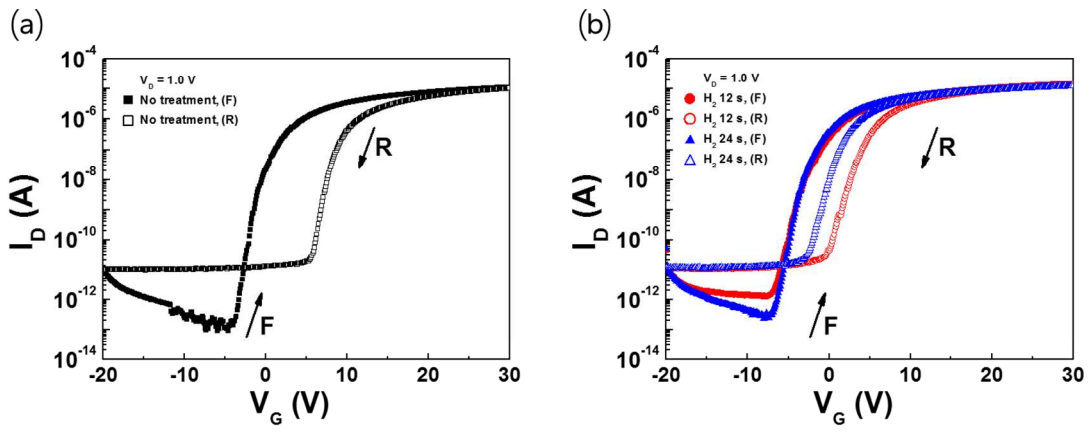

Figure S3. Transfer characteristics of TiO_2 MOSFETs with (a) no H_2-treatment and (b) under various H_2 treatment conditions, where F and R refer to forward and reverse directions, respectively.

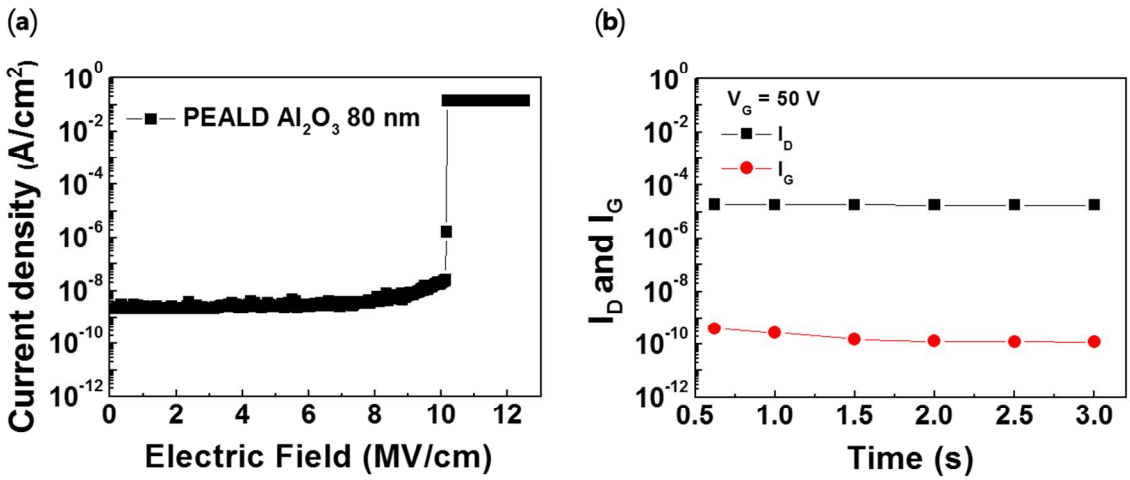

Figure S4 (a) breakdown characteristic curve of Al_2O_3 and (b) the gate current measured with the programming voltage of 50 V (L/W = 10 μm/40 μm).

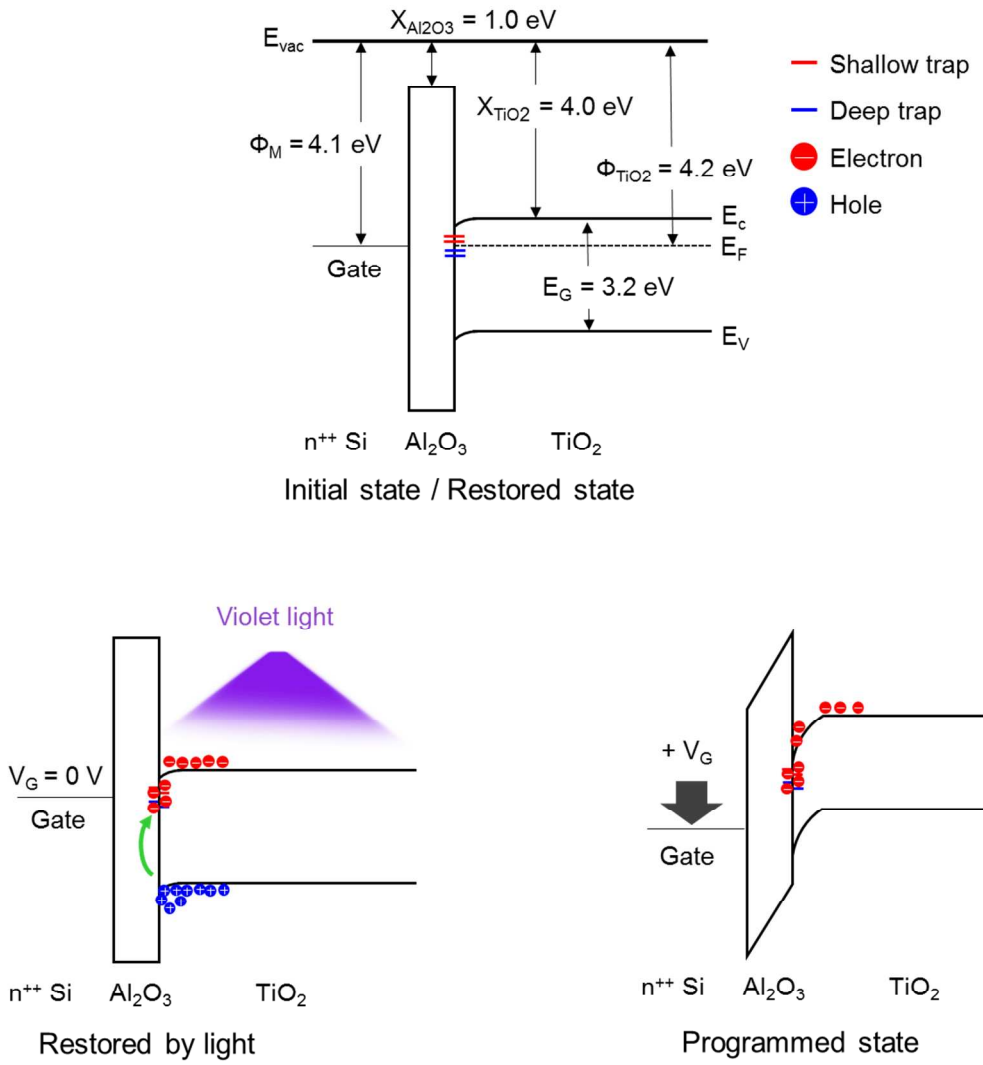

Figure S5. Schematic illustration of the mechanisms of the restoration procedure of the device, depicting the (a) initial state, (b) saturated state and (c) restoration by VL irradiation. (Φ_M : The work function of gate metal, Φ_{TiO2} : The work function of TiO_2, X_{Al2O3} : The electron affinity of Al_2O_3, X_{TiO2} : The electron affinity of TiO_2, E_G = Energy band gap, E_C = conduction band energy, E_F = Fermi energy level, E_V = valance band energy)

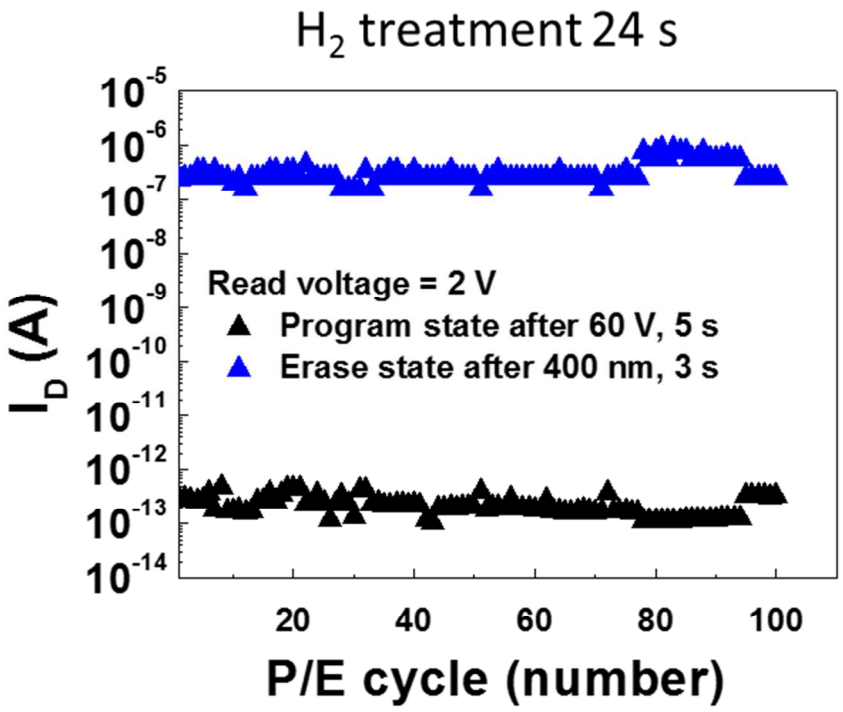

Figure S6. Program/erase (P/E) cycling tests of the TOFDI TiO_2 memory showing high reliability.

Supplementary references

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