Supplementary Information

In Situ Observation of Resistive Switching in an Asymmetric Graphene Oxide Bilayer Structure

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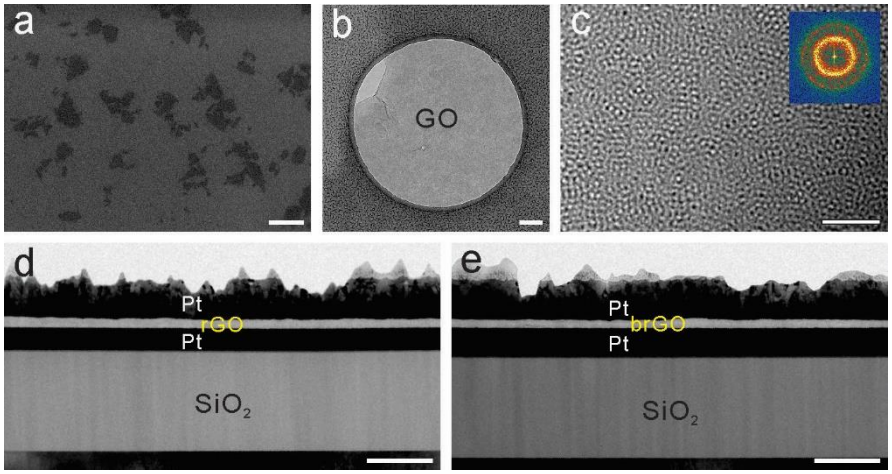

Figure S1. Characterization of GO films. (**a**) Scanning electron microscopy (SEM) image of GO sheets dispersed in deionized water (scale bar: 500 nm). (**b**) TEM image of GO films transferred on an Au quantifoil grid (scale bar: 200 nm). GO thin films were fabricated on SiO_2 wafer using spin coating method, and SiO_2 layer was etched using buffer oxide etchant. The rinsed GO films were transferred to an Au grid. (**c**) Atomic resolution TEM image of the transferred GO films. GO sheets show a significant number of defect sites which can be bonded to oxygen ions (scale bar: 2 nm). The right inset is FFT patterns obtained from (c). Cross-sectional TEM images of (**d**) Pt/rGO/Pt and (**e**) Pt/brGO/Pt memory devices (scale bar: 200 nm). Each of GO films were uniformly formed between two Pt electrodes using spin coating method.

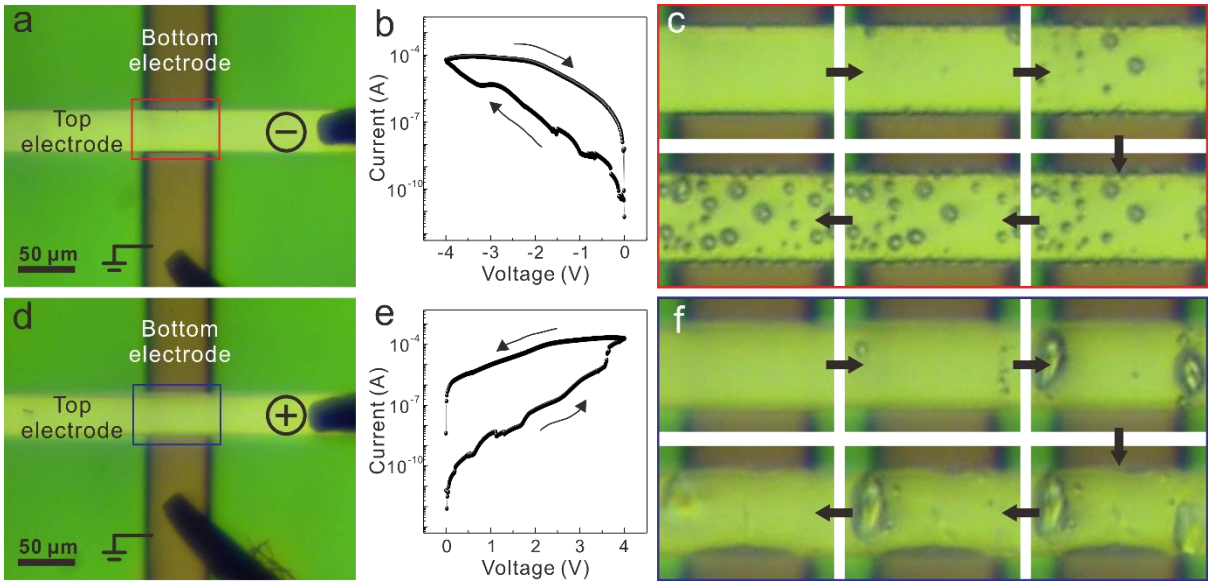

Figure S2. Bubble formations in Pt/rGO/Pt devices during electrical bias sweeps. Optical microscopy images of crossbar type memory device before (**a**) the negative bias sweep and (**d**) the positive bias sweep. Typical I-V curve of Pt/rGO/Pt memory device plotted on a semilogarithmic scale during (**b**) the negative sweep and (**e**) the positive sweep. The bias was applied along the arrows. (**c**) and (**f**) show optical images during bias sweeps obtained from the red and blue rectangular regions in (a) and (d), respectively. The bubbles were formed at the edge of the top electrode at an early stage when the native bias was applied to the top electrode, and it propagated to the surface of the top electrode. When the positive bias was applied to the top electrode, the bubbles were generated at the cross region between the edge of the bottom electrode and the top electrode.

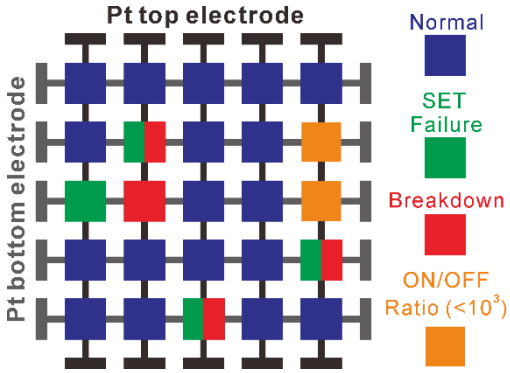

Figure S3. Electrical properties of 5x5 crossbar array Pt/brGO/Pt devices. 18 cells (72 %) are normally operated except for 2 cells with a low on/off ratio of 10^3 (read voltage -1.0 V) and 5 cells showing non-switching characteristic, indicating that bilayer structure shows the improved resistive switching properties compared to rGO and hrGO films.

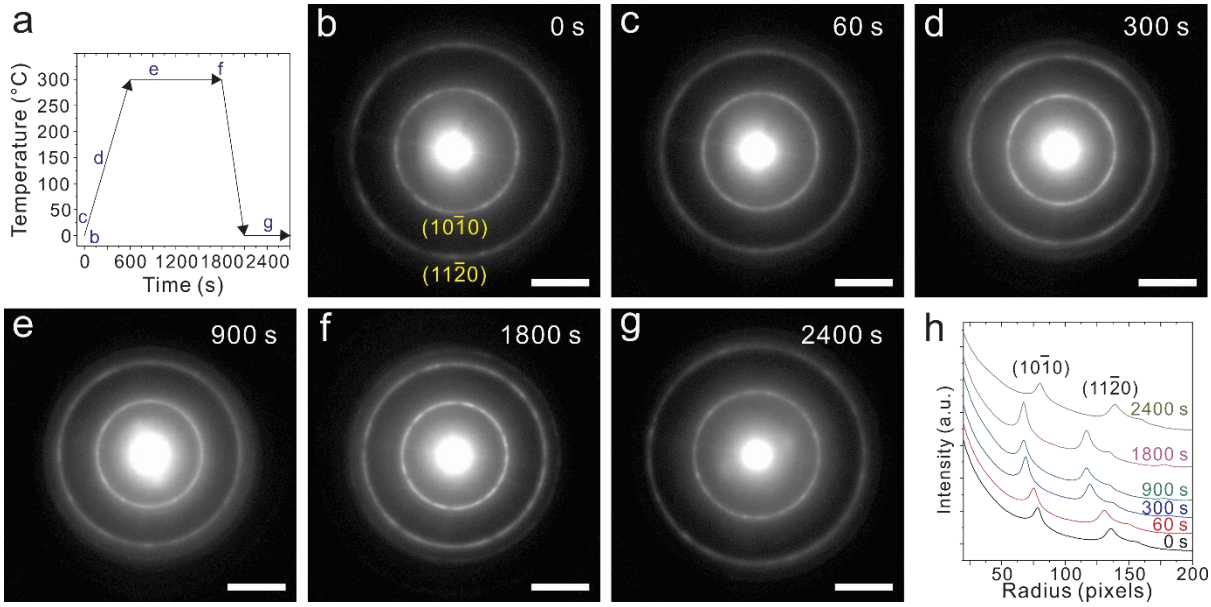

Figure S4. The thermal-induced lattice expansion of GO sheets (**a**) *In situ* heating experimental condition during 300 ℃ annealing process. Randomly stacked GO sheets on grid were heated to 30 ℃ per minute after 100 ℃ annealing process. The arrows show the change in temperature. (**b**-**g**) In situ TEM images of ED patterns obtained from GO sheets during annealing process (scale bar: 5 1/nm). The lattice spacing of each plane increase due to the thermal expansion of GO sheets. (**h**) The intensity profiles of ED patterns using ImageJ. The profile plot of normalized integrated intensities around concentric circles as a function of distance from the center of transmission beam. The expanded lattice spacing caused by thermal expansion of GO sheets decreased while lowering the temperature. When the temperature is finally changed back to room temperature at 2400 s, the lattice spacing of the thermally reduced GO sheets at 300 ℃(g) is slightly lower than that of the reduced GO sheets at 100 ℃ (h).

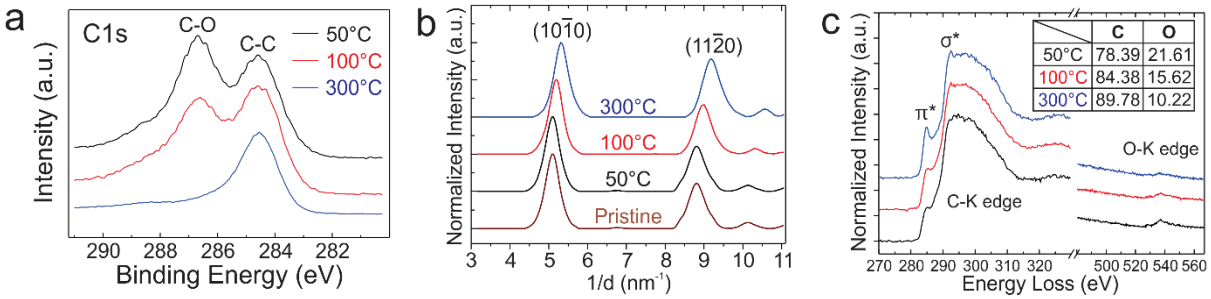

Figure S5. Characterization of thermally reduced GO films (**a**) XPS spectra of C 1s region with the different reduction process. (b) The intensity profiles of the radial distribution function (RDF) from the center to a desired radius using the ELD program in ED patterns form Figure 2(b). (c) EELS profiles of the C K edge and O K edge from rGO films at the elevated temperature.

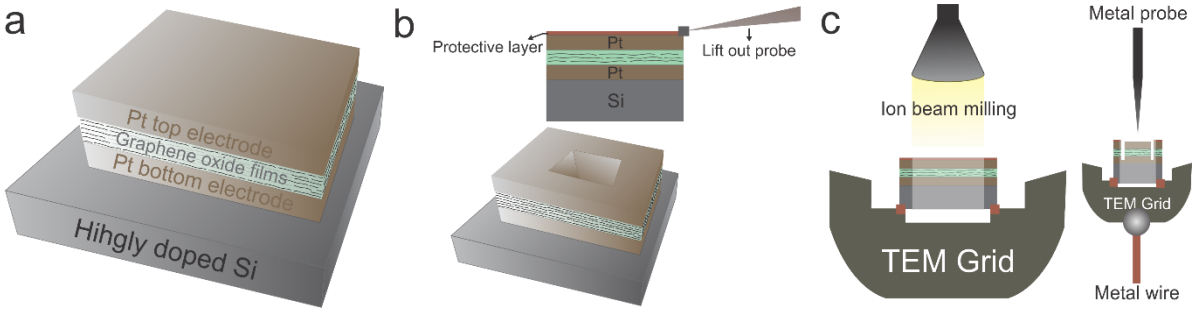

Figure S6. The sample preparation for *in situ* TEM observation. (**a**) Crossbar type Pt/brGO/Pt memory device was fabricated onto the highly-doped silicon wafer for forming the electrical contact. (**b**) The cross-sectional sample was cleaved using FIB equipment, and it was attached to the lift out probe. To minimize the ion beam damage, Pt protection layer was deposited on the top electrode. (**c**) The cleaved sample was connected to the TEM grid. The highly-doped silicon substrate was electrical connected to the grid. The mounted sample was additionally sharpened by Ga ion beam. The top electrode was isolated to prevent the direct contact between two electrodes caused by ion beam damage. The metal wire was bonded to sample-mounted TEM grid using conductive epoxy and silver paste.

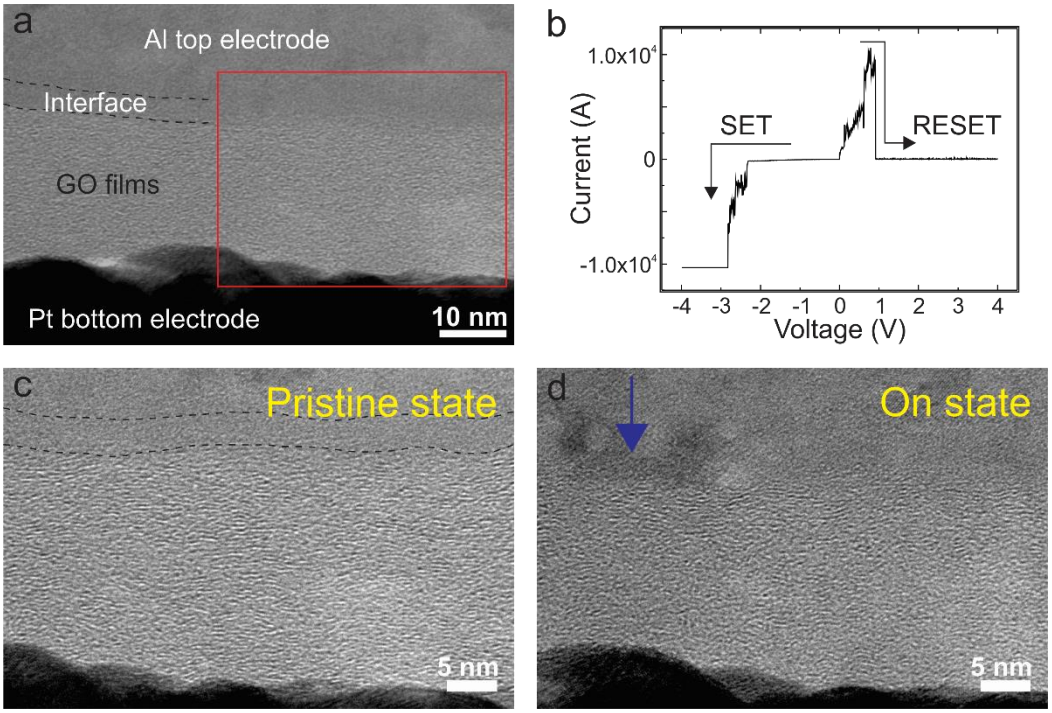

Figure S7. The reversible switching behaviour of an Al/rGO/Pt device. (**a**) Cross-sectional TEM image of the pristine state. An amorphous interface layer was formed by chemical reaction between Al top electrode and rGO films. (**b**) I-V curves of an Al/rGO/Pt memory device during in situ TEM observation. The bias was applied along the arrow. (**c**-**d**) Real-time TEM images capturing the metallic filament formation during the set state.

Movie S1. In situ observation of ED patterns in GO films under heat treatment. The temperature was elevated at 30℃/min. from the room temperature to 100 ℃ using heating holder. The first bright ring and the second ring indicate $(101\bar{0})$ and $(112\bar{0})$ planes of GO, respectively.

Movie S2. In situ observation of the resistive switching behaviour of a Pt/brGO/Pt device. The negative bias was applied to the top Pt electrode. The thickness of brGO films was reduced, and the microstructure changes of brGO films was simultaneously observed.

Movie S3. In situ observation of the resistive switching behaviour of an Al/rGO/Pt device. The negative bias was applied to the top Al electrode. The arrows indicate the filament regions where an amorphous interface layer changes to Al metallic channel.