Supplementary Information for:

Graphene-Quantum Dot Hybrid Optoelectronics at Visible Wavelengths

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Supplementary Movie Captions:

Movie S1: Gate-controlled fluorescence of colloidal QDs:

Fluorescence images of QDs embedded in the dielectric layer of an ambipolar graphene transistors as the gate voltage varies from -40 V to 45 V. The gate voltage is shown in the top left corner. The movie shows that the fluorescence of QDs is quenched at the positive and negative gate voltages. The blinking of QDs is also noticeable in the movies.

Movie S2: Gate-controlled fluorescence of colloidal QDs embedded in a p-type graphene transistors:

Fluorescence images of QDs embedded in the dielectric layer of a p-type graphene transistor as the gate voltage varies from -80 V to 80 V. The gate voltage is shown in the top left corner. The movie shows that the fluorescence of QDs is quenched at the negative gate voltages.

Movie S3: **Graphene based fluorescence display**:

Fluorescence images of static chessboard pattern generated by 5x5 passive matrix graphene display as the voltage difference between the top and bottom electrodes varies from -20 V to 20 V. The supply voltage is shown in the top left corner. The movie shows that to generate a considerable fluorescence contrast, the voltage difference should be larger than 10 V.

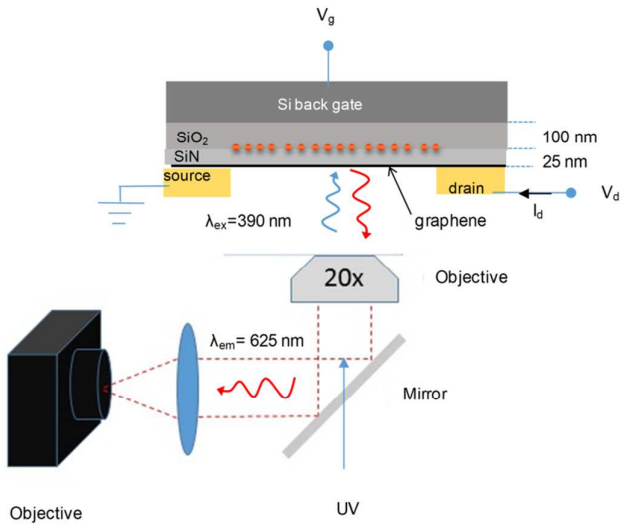
Movie S4: Dynamic fluorescence images generated by the display device:

Real time dynamic fluorescence images generated by the display device. The image is generated by applying -10 V bias to the data lines (the rows) while scan circuit applies +10V to a single column and moves the column from left to right for every second.

Movie S5: Dynamic fluorescence images generated by the display device:

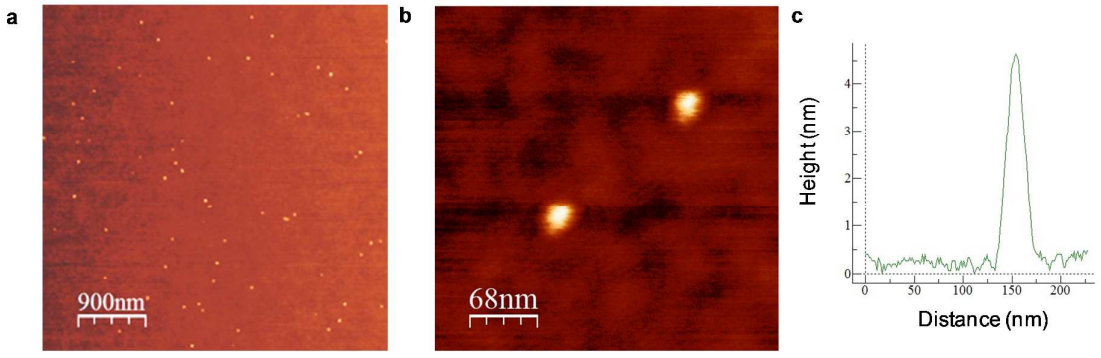
Real time dynamic fluorescence images generated by the display device. The image is generated by applying -10 V bias to the data lines (the rows) while scan circuit applies +10V to a single column and moves the column from left to right for every 200 ms.

Schematic representation of the optical set up:



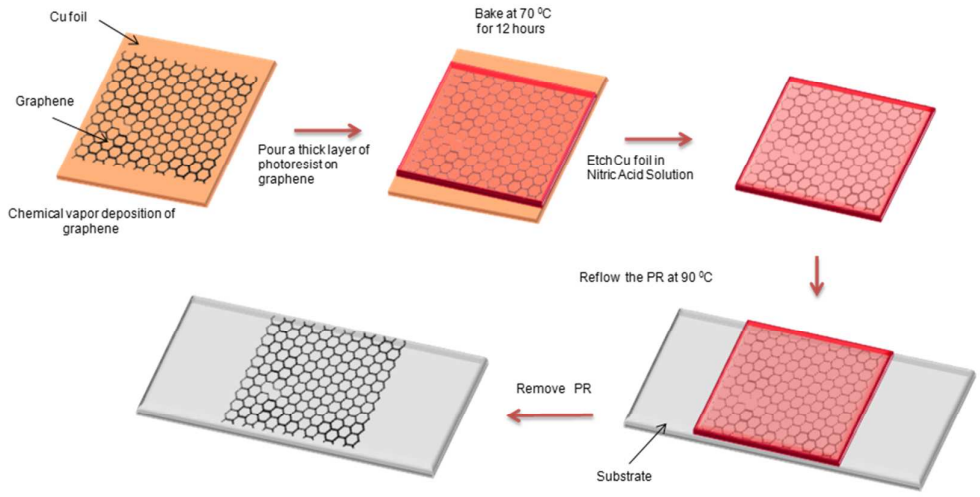
SFigure 1. Schematic representation of the optical set up used to measure fluorescence intensity of the QDs integrated with graphene. The applied gate voltage modulates the intensity of the fluorescence. The objective collects emitted light from the QDs, and then sends collected light into a CCD camera.

Atomic force microscope images of colloidal quantum dots:



SFigure 2. (a-b) Atomic force microscope images and, (c) cross-section profiles of QDs coated on Si_3N_4 dielectric using drop casting technique. The average diameter of QDs is around 6 nm. The QD-graphene distance includes the thickness of the dielectric and the radius of the QD.

Transfer-printing process and fabrication steps:



SFigure 3. The steps of transfer-printing process of graphene.

After the synthesis of graphene on ultra-smooth copper foils, we used the transfer-printing

1. Drop coat a thick photoresist layer (AZ5214) on the graphene coated surface of the copper.
2. Dry the sample in a preheated oven at 70 ^{0}C for 12 hours.
3. Put the sample facing copper side down on a nitric acid solution to etch copper substrate completely.
4. Rinse with DI water.
5. Dry with the samples N_2 gas flow.
6. Put photoresist-graphene layer on the targeted dielectric substrate with graphene side facing down.
7. Bake for 2 minutes on hot plate at 80 ^{o}C.
8. Bake for 2 minutes on hot plate at 120 ^{o}C.
9. Soak sample in acetone to remove photoresist.
10. Clean sample with acetone, isopropanol and DI water then dry with N_2flow.

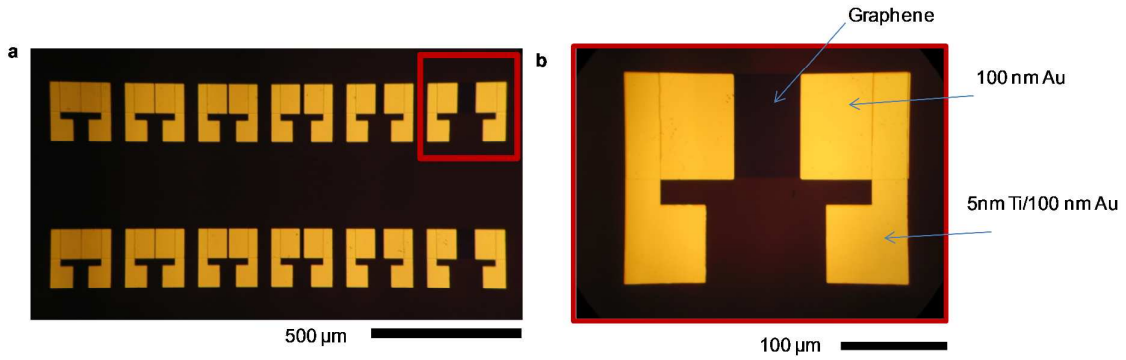
Deposition of gate dielectric:

In this work, for the fabrication of transistors, we used two dielectric layers; the gate dielectric and the spacer. The gate dielectric is deposited on Si wafers at 250 ^{0}C. Plasma enhanced chemical vapor deposition (PECVD) was used to grow stress free silicon nitrate (Si_3N_4) film on samples as the gate dielectric. Growth of Si_3N_4 film was carried out in PlasmaLab 8510C reactor at 250 ^{0}C and the process was carried out under the pressure of 1 Torr and RF power of 9 W. Flow rate was 200 sccm SiH_4 in H_2, 4 sccm NH_3, 50 sccm He, 35 sccm N_2. The film stress was +5MPa (tensile), growth rate was 8.4 nm/min and refractive index was 1.89.

Deposition of spacer dielectric:

Since spacer was deposited after coating the QD drop, we used room temperature PECVD deposition to prevent QDs to degrade from high temperature. The spacer deposition was carried out in PlasmaLab 8510C reactor at 27 ^{0}C (room temperature) and the process was carried out under the pressure of 1 Torr and RF power of 9 W. Flow rate was 200 sccm SiH_4 in H_2 and 20 sccm NH_3. Growth rate was 16 nm/min.

Graphene field effect transistors integrated with QDs and fabrication steps:



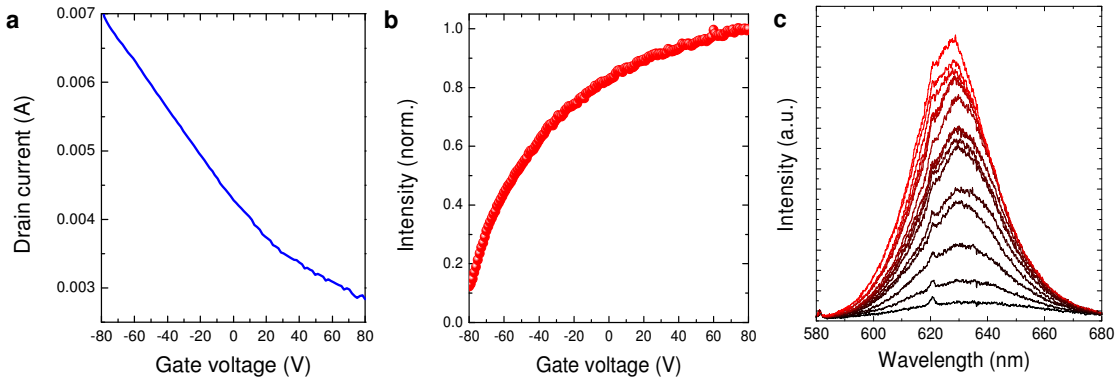
SFigure 4. (a) Optical microscope images of the fabricated graphene field effect transistors. (b) Optical microscope of an individual transistor. The source and drain electrodes were fabricated by two layers of metallization. In the first step, we deposited 100 nm Au on graphene without any adhesive layers. In the second step, we form the contact pads using 5nm Ti and 100 nm Au.

1. **Fabrication steps of graphene FET integrated with QDs:**

1. Deposit 65 nm Si_3N_4 gate dielectric on Silicon (100) wafer.
2. Drop cast QDs with the emission wavelength of 625 nm.
3. Deposit 25 nm Si_3N_4 spacer dielectric.
4. Transfer a graphene layer by using transfer-print method.
5. Use standard photolithograph to have contact patterns on the sample.
6. Evaporate 50 nm gold on the sample.
7. Soak sample in acetone for liftoff.
8. Use standard photolithography to pattern graphene channels.
9. Use RIE with 20 sccm O_2 flow and 20 µBar pressures to etch graphene.
10. Clean sample with acetone, isopropanol and DI water then dry with N_2 gas flow.
11. Use standard photolithograph to pattern contact pads for bonder.

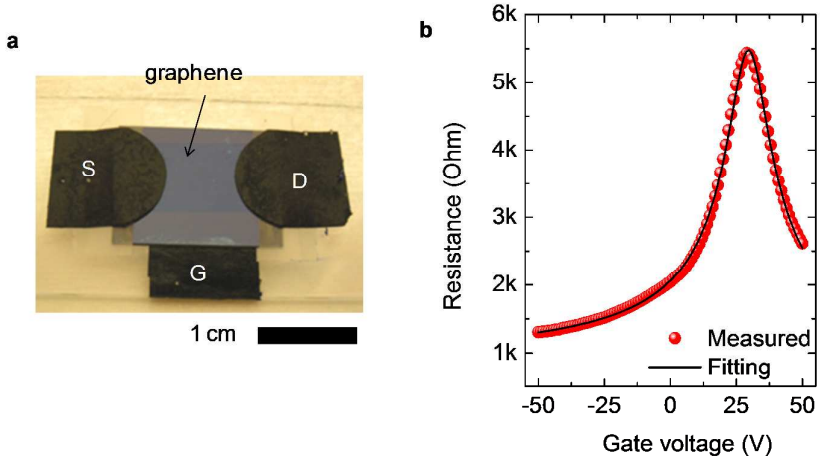
12. Sputter 5 nm Ti and evaporate 200 nm Au on the sample.
13. Soak sample in acetone for liftoff.
14. Dice sample into smaller pieces.
15. Stick sample to the sample holder with carbon tape.
16. Use bonder to make connections between sample and sample holder with 12 μm gold wire.

Gate-controlled fluoresce quenching for a p-type graphene transistor:



SFigure 5. (a) Transfer curve for a p-type graphene transistor with 100 nm thick SiO_2 gate dielectric and 25 nm Si_3N_4 spacer. (b) Normalized fluorescence intensity versus gate voltage. (c) Spectrum of the emission of QD when the gate voltage varies from -80 V to 80 V.

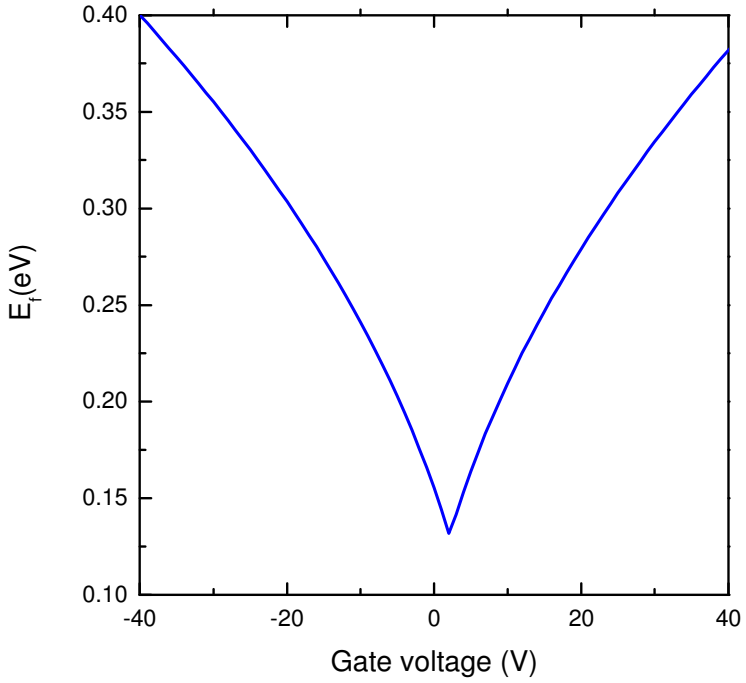
Large area graphene transistors and fabrication steps:



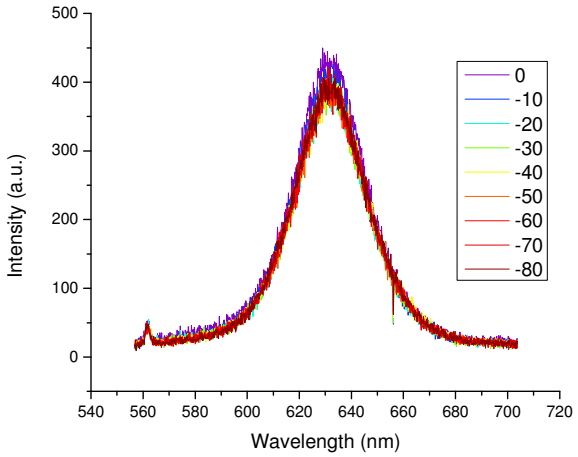
SFigure 6. (a) Image of a large area graphene transistor used for time resolved measurements. Conductive carbon tapes were uses to contact graphene layer. (b) The gate-dependent electrical resistance of the large area transistor with 90 nm gate dielectric (65 nm bottom dielectric and 25 nm top spacer). The resistance has a maximum value at the charge neutral point V_{CNP}=29 V. The on-off ratio of the transistor is around 5. The solid red line shows the fitting curve, which yields a minimum charge density of $2x10^{12}$ cm^{-2}.

Fabrication steps for large area scale graphene transistors used for time-resolved measurements:

1. Deposit 65 nm Si_3N_4 dielectric on highly doped Si (100) wafer.
2. Drop cast QDs with the emission wavelength of 625 nm.
3. Deposit 25 nm Si_3N_4 spacer dielectric using chemical vapor deposition at room temperature.
4. Transfer graphene layer by using transfer-print method.
5. Stick the sample to the glass slide with carbon tape to have gate connection.
6. Isolate the edges of the sample to prevent gate-leakage.
7. Apply the conductive carbon tape on both side of the large area graphene.

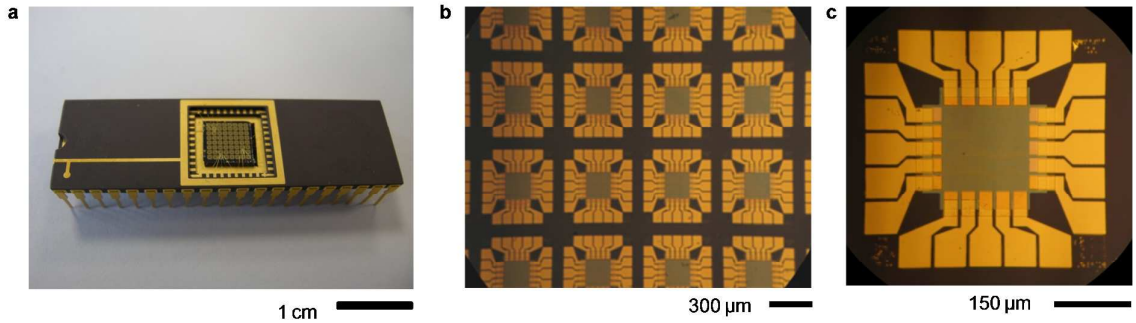


SFigure 7. Calculated Fermi energy as a function of gate voltage for the device whose electrical performance is given in Fig. 2c.



SFigure 8. Control experiments using ITO electrodes instead of graphene. Fluorescence intensity of the QDs integrated ITO electrodes at different gate voltages. We fabricated field effect transistors using 25 nm thick ITO as the channel materials. The device structure is the same with graphene-QD devices. The inset shows the applied gate voltages. We do not observe a significant modulation in the fluorescence intensity with the gate voltage. The variation in the spectra is due to the blinking of QDs.

The fabricated display device and fabrication steps:



SFigure 9. (a) The fabricated display devices wire bonded on a ceramic chip holder. (b) Optical microscope images of an array of display devices and, (c) an individual display device.

Fabrication steps of passive matrix graphene fluorescence display:

1. Deposit 300 nm Si_3N_4 dielectric on Silicon (100) wafer.
2. Transfer bottom graphene layer by using transfer-print method.
3. Use standard photolithograph to have contact patterns on the sample.
4. Evaporate 50 nm gold on the sample.
5. Soak sample in acetone for liftoff.
6. Use standard photolithography to pattern vertical graphene ribbons.
7. Use RIE with 20 sccm O_2 flow and 20 μBar pressures to etch graphene.
8. Clean sample with acetone, isopropanol and DI water then dry with N_2 gas flow.
9. Deposit 25 nm Si_3N_4 spacer dielectric.
10. Drop cast QDs with the emission wavelength of 625 nm.
11. Deposit 25 nm Si_3N_4 spacer dielectric.
12. Use standard photolithography to pattern Si_3N_4 film to remove dielectric from top of the contacts.
13. Etch Si_3N_4 inside buffered HF solution.
14. Transfer top graphene layer by using transfer-printing method.
15. Use standard photolithograph to have contact patterns on the sample.
16. Evaporate 50 nm gold on the sample.
17. Soak sample in acetone for lift-off process.
18. Use standard photolithography to pattern horizontal graphene ribbons.
19. Use RIE with 20 sccm O_2 flow and 20 μBar pressures to etch graphene.
20. Clean sample with acetone, isopropanol and DI water then dry with N_2 gas flow.
21. Use standard photolithograph to pattern contact pads for bonder.
22. Sputter 5 nm Ti and evaporate 200 nm Au on the sample.
23. Soak sample in acetone for liftoff.

24. Dice sample into smaller pieces.
25. Stick sample to the sample holder with carbon tape.
26. Use bonder to make connections between sample and sample holder with 12 µm gold wire.

Fabrication steps for the voltage-controlled color-variable device:

1. Deposit 300 nm Si_3N_4 dielectric on Silicon (100) wafer.
2. Transfer bottom graphene layer by using transfer-print method.
3. Use standard photolithograph to pattern contact metals on the sample.
4. Evaporate 50 nm gold on the sample.
5. Soak sample in acetone for liftoff.
6. Use standard photolithography to pattern vertical graphene ribbons.
7. Use RIE with 20 sccm O_2 flow and 20 µBar pressures to etch graphene.
8. Clean sample with acetone, isopropanol and DI water then dry with N_2gas flow.
9. Deposit 25 nm Si_3N_4 spacer dielectric.
10. Drop cast QDs with the emission wavelength of 585 nm.
11. Deposit 75 nm Si_3N_4 spacer dielectric.
12. Use standard photolithography to pattern Si_3N_4 film to remove dielectric from top of the contacts.
13. Etch Si_3N_4using buffered HF solution.
14. Transfer middle graphene layer by using transfer-print method.
15. Use standard photolithograph to have contact patterns on the sample.
16. Evaporate 50 nm gold on the sample.
17. Soak sample in acetone for liftoff.
18. Use standard photolithography to pattern horizontal graphene ribbons.

19. Use RIE with 20 sccm O_2 flow and 20 μBar pressures to etch graphene.
20. Clean sample with acetone, isopropanol and DI water then dry with N_2gas flow.
21. Deposit 75 nm Si_3N_4 spacer dielectric.
22. Drop cast QDs with the emission wavelength of 625 nm.
23. Deposit 25 nm Si_3N_4 spacer dielectric.
24. Use standard photolithography to pattern Si_3N_4 film to remove dielectric from top of the contacts.
25. Etch Si_3N_4using buffered HF solution.
26. Transfer top graphene layer by using transfer-print method.
27. Use standard photolithograph to have contact patterns on the sample.
28. Evaporate 50 nm gold on the sample.
29. Soak sample in acetone for liftoff.
30. Use standard photolithography to pattern horizontal graphene ribbons.
31. Use RIE with 20 sccm O_2 flow and 20 μBar pressures to etch graphene.
32. Clean sample with acetone, isopropanol and DI water then dry with N_2gas flow.
33. Use standard photolithograph to pattern contact pads for bonder.
34. Sputter 5 nm Ti and evaporate 200 nm Au on the sample.
35. Soak sample in acetone for liftoff.
36. Dice sample into smaller pieces.
37. Stick sample to the sample holder with carbon tape.
38. Use wire-bonder to make connections between sample and sample holder with 12 μm gold wire.