Supporting Information

High-Performance Flexible Single-Crystalline Silicon Nanomembrane Thin-Film Transistors with high-k Nb_2O_5-Bi_2O_3-MgO Ceramics as Gate Dielectric on a Plastic Substrate

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1. XRD and SEM for BMN ceramics films on PET substrate:

Figure S1 shows the SEM surface morphologies of BMN ceramics layers with different thickness (80 nm and 120 nm). No certain morphologies except a smooth surface can be observed from the SEM image in Figure S1. This result is in a good agreement with the analysis of XRD characteristics (all the gate layers are of an amorphous nature). However, the particle size in the surface gradually decreases with increasing the thickness of BMN gate layers, which indicate the surface roughness has been increased. The surface roughness would affect the electrical performance of the thin films.

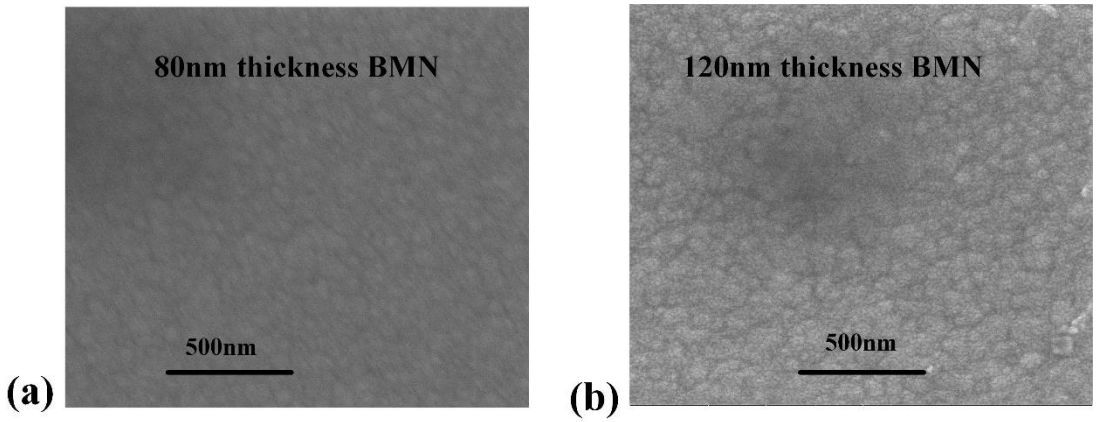

Figure S1. (a) SEM image for 80 nm BMN. (b) SEM image for 120 nm BMN.

2. Microscope images for the transferred SiNM and finished TFTs on PET substrate:

Figure S2(a) shows the transferred SiNM on PET substrate coated with BMN. A high transfer yield and flat surface of the transferred SiNM can be observed. Figure S2(b) shows the TFT arrays fabricated on flexible substrate with different dimensions. Figure S2(c) shows the microscope images for 30um/5um width/length TFTs where double-channel structure is employed.

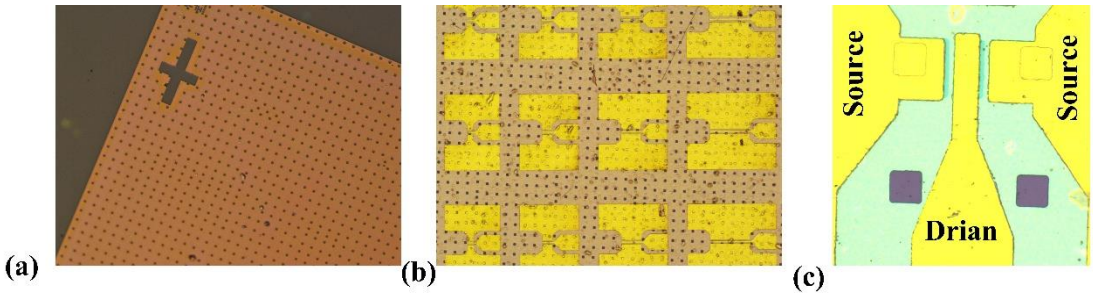

Figure S2. (a) Transferred SiNM on the flexible substrate coated with ITO and BMN layers. (b) Finished TFTs array on the PET substrate. (c) The microscope image of the flexible W/L=30um/3um TFT.

3. Schematic diagram for the flexible TFTs with definitions of channel width W and channel length L

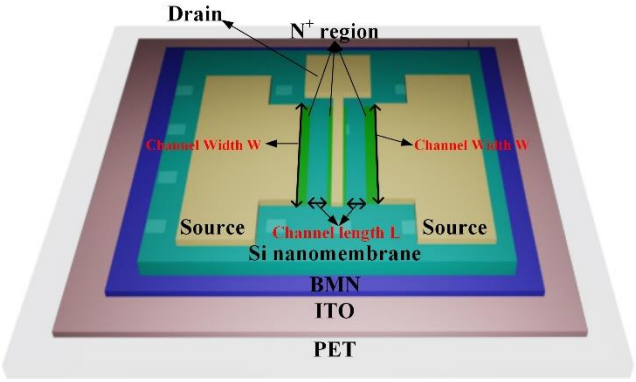

Figure S3. Schematic diagram for the flexible TFTs with definitions of W and L. As shown in Figure S3, W is the direction perpendicular to the current flow direction, and L is the direction paralleled to the current flow direction.

4. Performance for the flexible W/L=30μm/5μm device :

Figure S4(a) shows the linear transfer characteristics for the flexible 30um/5um TFT. Figure S4(b) shows the I-V characteristics of the flexible TFT. Gate voltage is from 1.5 V to 2.8 V and the drain voltage is from 0 V to 4 V.

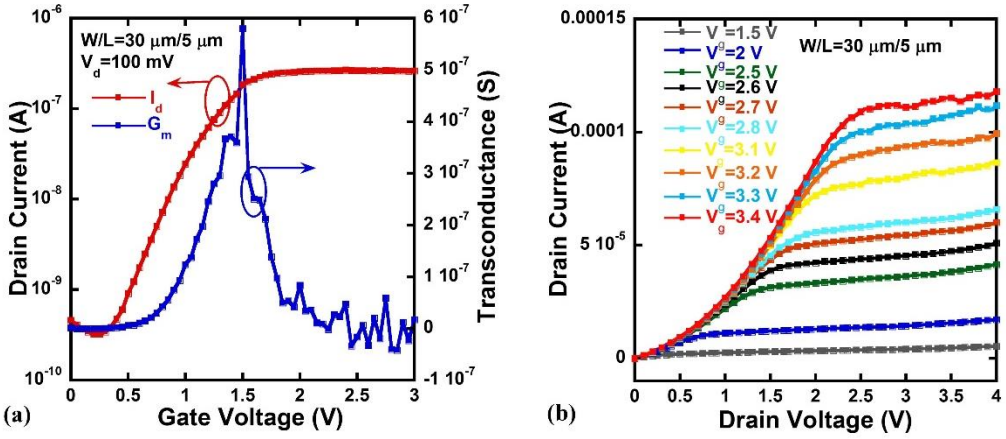

Figure S4. (a) Linear transfer characteristics for the flexible W/L=30 μm/5 μm device. (b) I-V characteristics for the flexible W/L=30 μm/5 μm device.

5. Bending strain calculations

The calculation schematic for bending strain is shown in Figure S5. The flexible TFTs are settled on the bending mould with a radius of R. The total thickness of the flexible TFTs is ΔR, which contains the PET substrate (~175 μm), BMN dielectric layer (~100 nm), Si nanomembrane (~200 nm) and the metal electrode (~130 nm). Because of the zero-strain plane in the middle for bent TFTs on plastic substrate, L is the reference length and can be calculated as

$$L = 2\pi(R + \frac{\Delta R}{2})\theta \qquad (1)$$

When the device is bended, the flexible nanomembrane on plastic substrate is under tensile strain condition, and has an L increment for L+ΔL and ΔL is the elongation. It can be expressed that

$$L + \Delta L = 2\pi(R + \Delta R)\theta \qquad (2)$$

So the tensile strain in the flexible TFT nanomembrane can be expressed

$$\text{Strain} = \frac{\Delta L}{L+\Delta L} = \frac{2\pi(R+\Delta R)\theta - 2\pi\left(R+\frac{\Delta R}{2}\right)\theta}{2\pi(R+\Delta R)\theta} = \frac{\Delta R}{2R+\Delta R} = \frac{1}{\left(\frac{2R}{\Delta R}\right)+1} \qquad (3)$$

This equation can be used to calculate the bending strains.

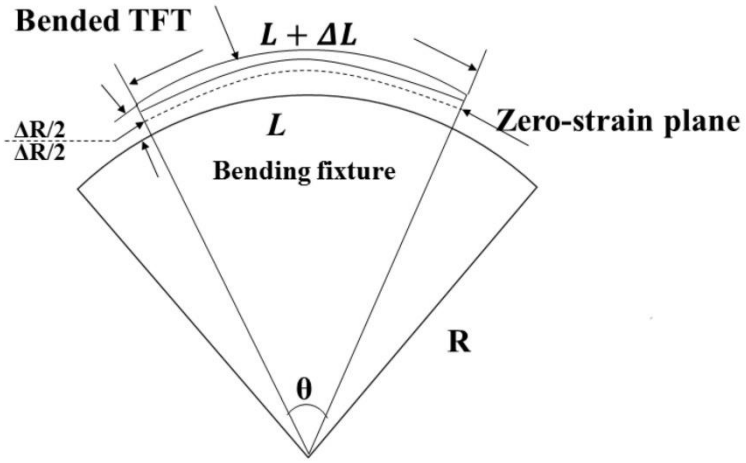

Figure S5. Schematic of bending strain calculations for flexible TFTs.

6. Equivalent circuit model and model calculations for the bending devices:

To better understand the device performance on flat state, an equivalent circuit model has been built. Figure S6(a) shows the detailed equivalent circuit model for devices with equivalent parasitic resistance and capacitance. The model is put into ADS for calculations. Figure S6(b) shows the comparison results under flat. The model calculations have good agreement with the experimental results, and the associated device parameters have been extracted.

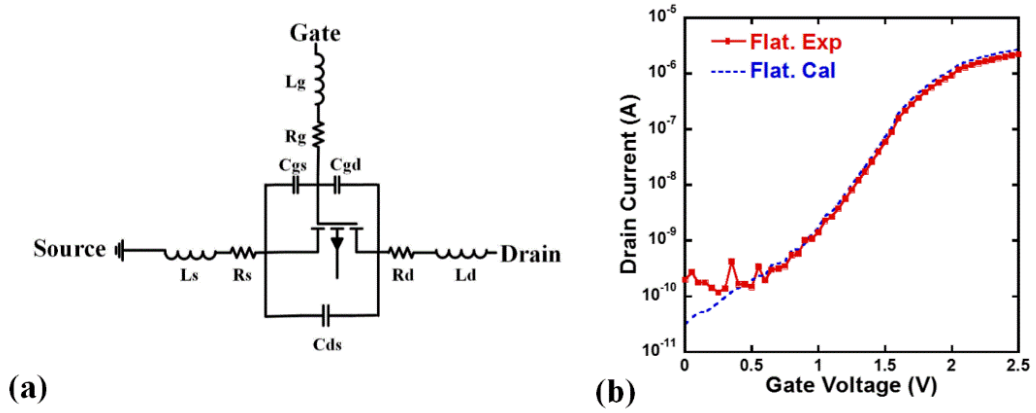

Figure S6. (a) Equivalent circuit model for the flexible SiNM TFTs. (b) Comparison of the model calculation results and measured data for the flexible TFTs at flat state.