Supporting Information

Localized Electrothermal Annealing with Nanowatt Power for a Silicon Nanowire Field-Effect Transistor

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1. Schematics of the fabrication process flow, and taken images.

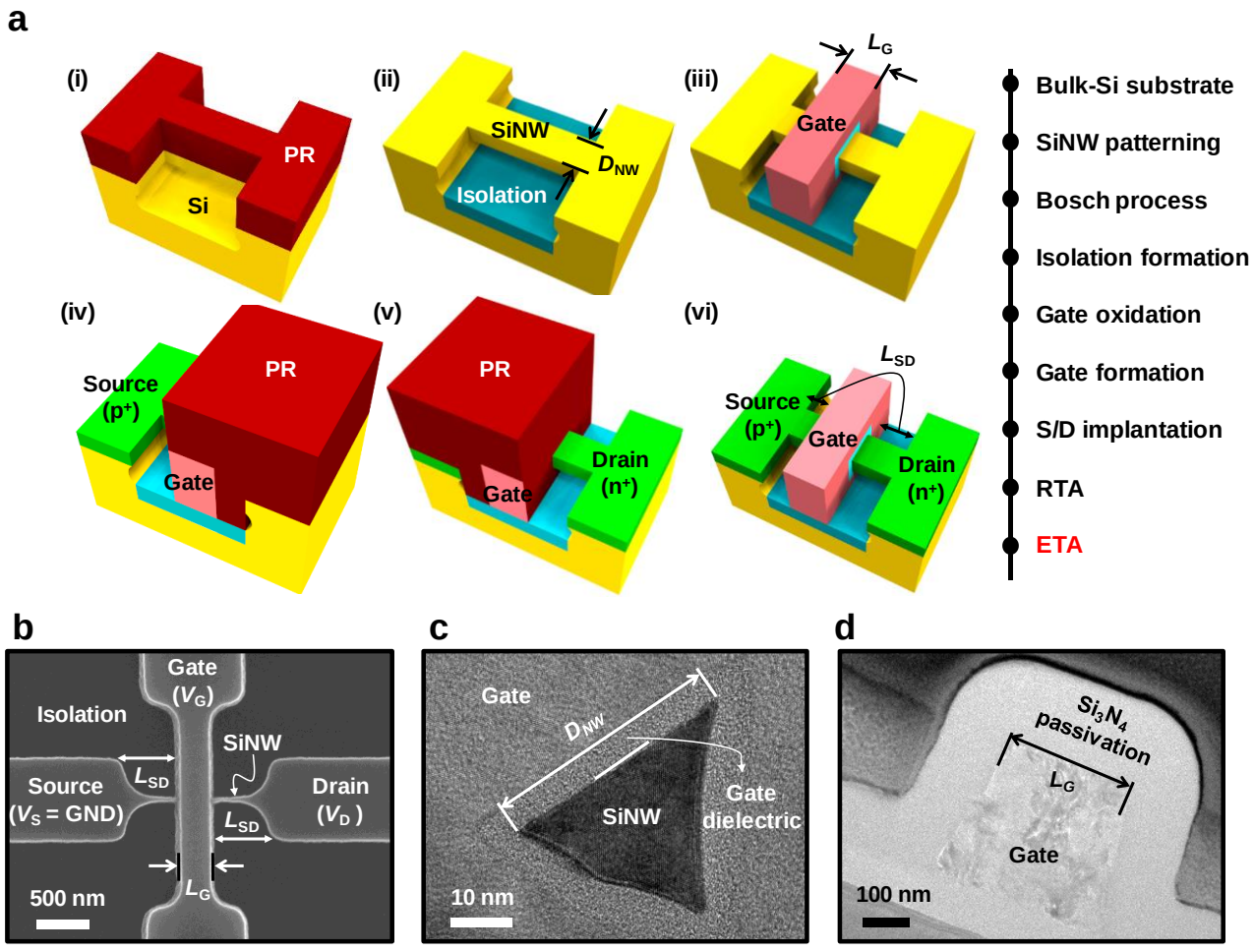

Figure S1. (a) (i) Isotropic reactive-ion dry etching (Bosch process: C_4F_8 and SF_6). (ii) TEOS deposition, chemical-mechanical planarization (CMP), and wet recessing. (iii) Gate oxidation, n^+ poly-Si deposition, and patterning for gate formation. (iv-v) Masking and ion implantation for source (B: 5 keV, $5x10^{15}$ cm^{-2}) and drain (As: 10 keV, $5x10^{15}$ cm^{-2}) formation. (vi) PR removing, RTA, and ETA. (b) A scanning electron microscope (SEM) image of the fabricated platform device. c, Cross-sectional transmission electron microscope (TEM) images of the fabricated device along the gate (d), and the SiNW. The length of the intrinsic region, which corresponds to the gate length (L_G), is 300 nm, and the diameter (D_{NW}) of the SiNW is 45 nm. The length of the source and drain region (L_{SD}) is 500 nm.

2. Power consumption and thermal budget of the various kinds of annealing.

Table S1. Comparison of the various kinds of annealing.

Type	**Heat Source**	**Power (W)**	**Time (sec)**
Rapid thermal annealing (RTA[S1])	halogen lamp	10^3	1
Laser annealing (LSA[S2])	laser	$10 \sim 10^3$	10^{-9}
Electrothermal annealing[S3]	Drift current	12 mW	10^{-3}
Electrothermal annealing[S4]	Drift current	3 mW	10^3
Electrothermal annealing[S5]	Drift current	0.68 mW	10^{-4}
This work	Tunneling current	370 nW	10^{-4}

3. Time dependency of the I_{ON} after ETA

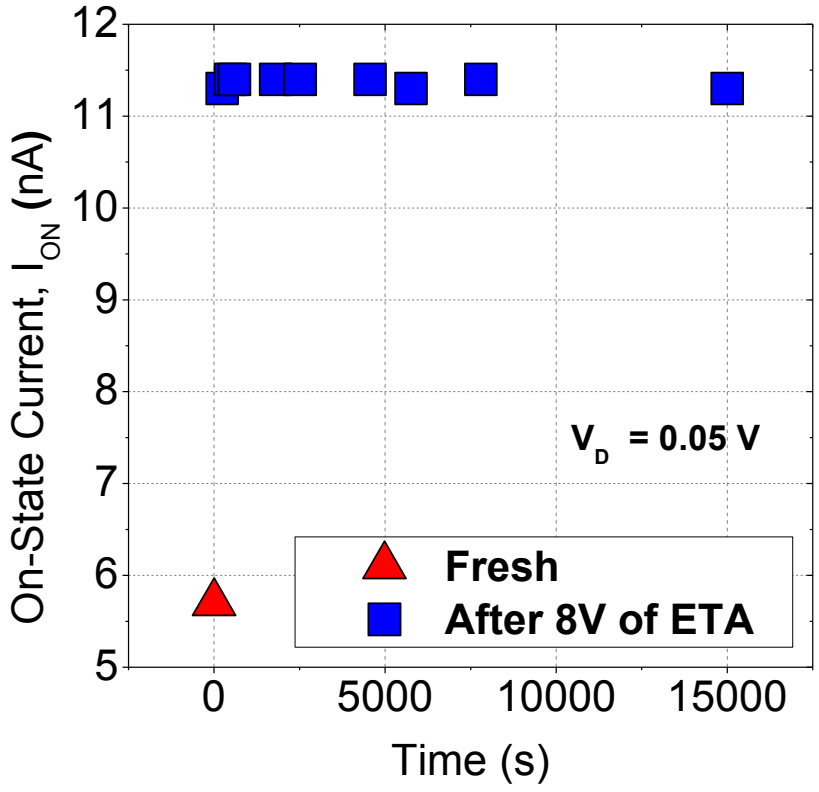

Figure S2. Measured I_{ON} of the device after V_{ETA}. The improved performance is remained without degradation.

4. Dopant activation-induced ambipolar characteristics at the drain

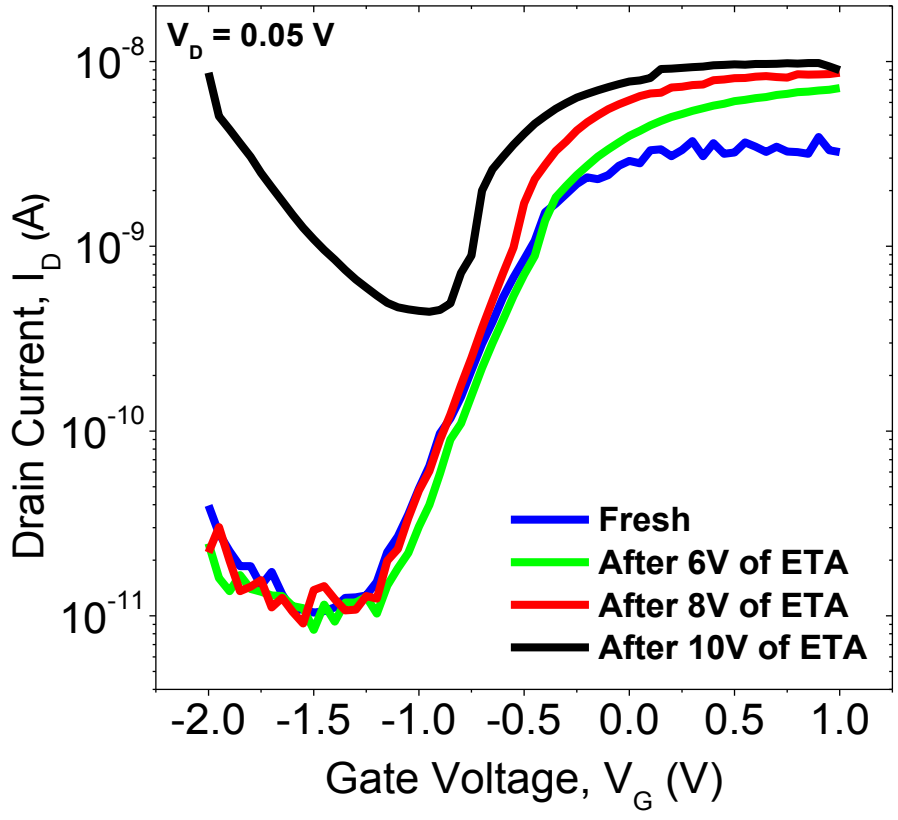

Figure S3. Measured I_D-V_G characteristics of the device after excessive V_{ETA}. The I_{OFF} is increased due to the tunneling of the electrons from the intrinsic region to the drain.

It is noticeable that the increase in the I_{OFF} is related to the ambipolar characteristics of the device, as shown by the blue line in Figure S3. In general, the source and drain of the TFET are sufficiently activated by utilizing global thermal annealing methods. However, the thermal process cannot anneal the source and drain selectively. Hence, the increment in the I_{OFF} caused by the tunneling effect near the drain, is considered to be one of the challenging issues in the field of electron devices. This increment in I_{OFF} can be reduced by several drain engineering, such as gate to drain overlap[S6], low doping concentration[S7], and large bandgap material.

5. Extracted resistance of the source and drain before and after ETA

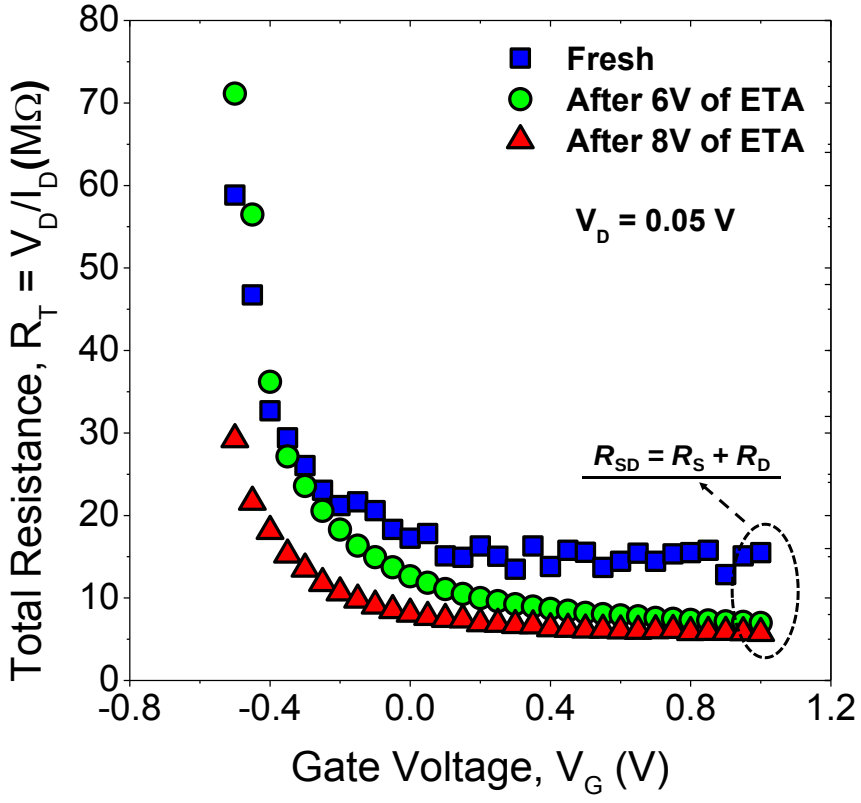

Figure S4. Extracted R_{SD} before and after ETA by extrapolation of the total resistance of R_T.

Based on the measured I_D-V_G in Figure 2a, a simple extraction method was applied to extract the R_{SD} (= R_S + R_D) of the device[S8] as shown in Figure S4. The extracted R_{SD} was 15.4 MΩ in a fresh device, but the resistance was reduced to 6.15 MΩ after 8V of ETA.

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S5. Park, J.-Y.; Hur, J.; Choi, Y.-K. Demonstration of a Curable Nanowire FinFET using Punchthrough Cu rrent to Repair Hot-Carrier Damage. *IEEE Electron Devices Lett.*, In press.

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S7. Krishnamohan, T.; Kim, D.; Raghunathan, S.; Saraswat, K. Double-Gate Strained-Ge Heterostructure Tunneling FET (TFET) With record high drive currents and ≪60mV/dec subthreshold slope. *IEEE International Electron Devices Meeting* **2008**, 1–3.

S8. Campbell, J. P.; Cheung, K. P.; Suehle, J. S.; Oates, A. Simple Series Resistance Extraction Methodology for Advanced CMOS Devices. *IEEE Electron Device Lett.* **2011**, 32, 1047–1049.