Supporting Information

Photo-Thermally Activated Nanocrystalline Oxynitride with Superior Performance in Flexible Field-Effect Transistors

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Fabrication of flexible devices. The nc-ZnO_xN_y TFTs (bottom gate and bottom contact structure, BGBC) were fabricated on PEN films with carrier glass substrate by the conventional photolithography method. The processing temperature was fixed at 175 ^oC. Cooling-off type adhesive film was added between the PEN and the glass substrate. After the laminating process, the cleaning process was conducted using isopropyl alcohol (IPA) and deionized (DI) water sequentially for 10 min each in the sonicator bath, and, then, pre-baking done at 150 ^oC for 3 min. Organic/inorganic (polysilsesquioxane/Al_2O_3) hybrid buffer layers were deposited on the PEN substrate to provide a smooth, flat surface and to restrain gas diffusion from water and oxygen molecules. The 100 nm-thick ITO film used as the gate electrode was patterned by wet-etch process heated up to 40 ^oC. Using the atomic layer deposition (ALD) process, the 100 nm-thick Al_2O_3 film was deposited at 150 ^oC, and, then, the contact pad via the gate electrode was patterned by phosphoric acid at 140 ^oC. The 100 nm-thick ITO film was patterned as the S/D electrode, which had channel width and length of 40 and 40 μm, respectively. The 15 nm-thick nc-ZnO_xN_y film was formed by an identical DC reactive sputtering method and post TPC treatment. In order to prevent chemical damage during the lithography process, a 10 nm-thick Al_2O_3 film was deposited as a protective layer using the ALD process at 150 ^oC. The active/protective layers were patterned by dilute hydrofluoric acid at the same time. After cooling the substrate at $< \sim 0$ ^oC ambient, the delamination process of the flexible nc-ZnO_xN_y TFTs from carrier glass was conducted by the mechanical rolling method (radius, R = 15 mm).

Table S1. Threshold voltage shift (ΔV_{th}) for negative and positive gate bias stress as a function of stress time.

LT-treated ZnO_xN_y TFT			TPC-treated ZnO_xN_y TFT		
Stress time (s)	$\Delta V_{th, NBS}$ [a] (V)	$\Delta V_{th, PBS}$ [b] (V)	Stress time (s)	$\Delta V_{th, NBS}$ (V)	$\Delta V_{th, PBS}$ (V)
0	631.62	189.5	0	22.2	5390.9
32	946	126.5	32	250	478.7
100	945.33	126.6	100	22.6	5295.5
317	493.3	242.6	317	480.7	249.0
1000	682.8	175.3	1000	305	392.4
3600	493.8	242.4	3600		

[a] ΔV_{th} for negative gate bias stress (V_G =-20 V),

[b] ΔV_{th} for positive gate bias stress (V_G =20 V)

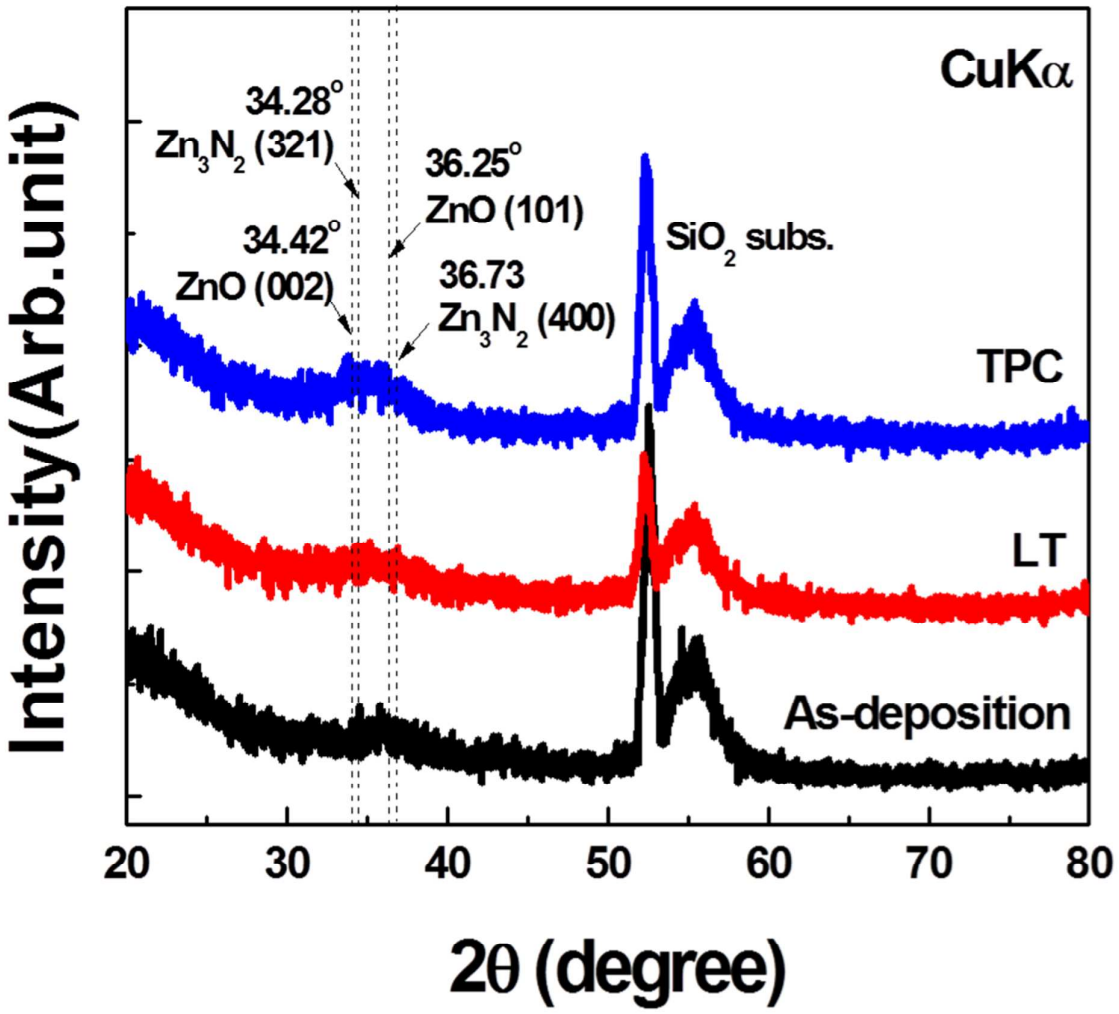

Figure S1. X-ray diffraction spectra of As-deposition, LT-, and TPC-treated ZnO_xN_y films on SiO_2 substrate measured by the glancing incident x-ray diffraction (GIXRD) method. The fixed angle (ω) = 0.5°, and the mixed phase of ZnO (101), (002) and Zn_3N_2 (321) and (400) are shown in the broad range of 33 – 37°.

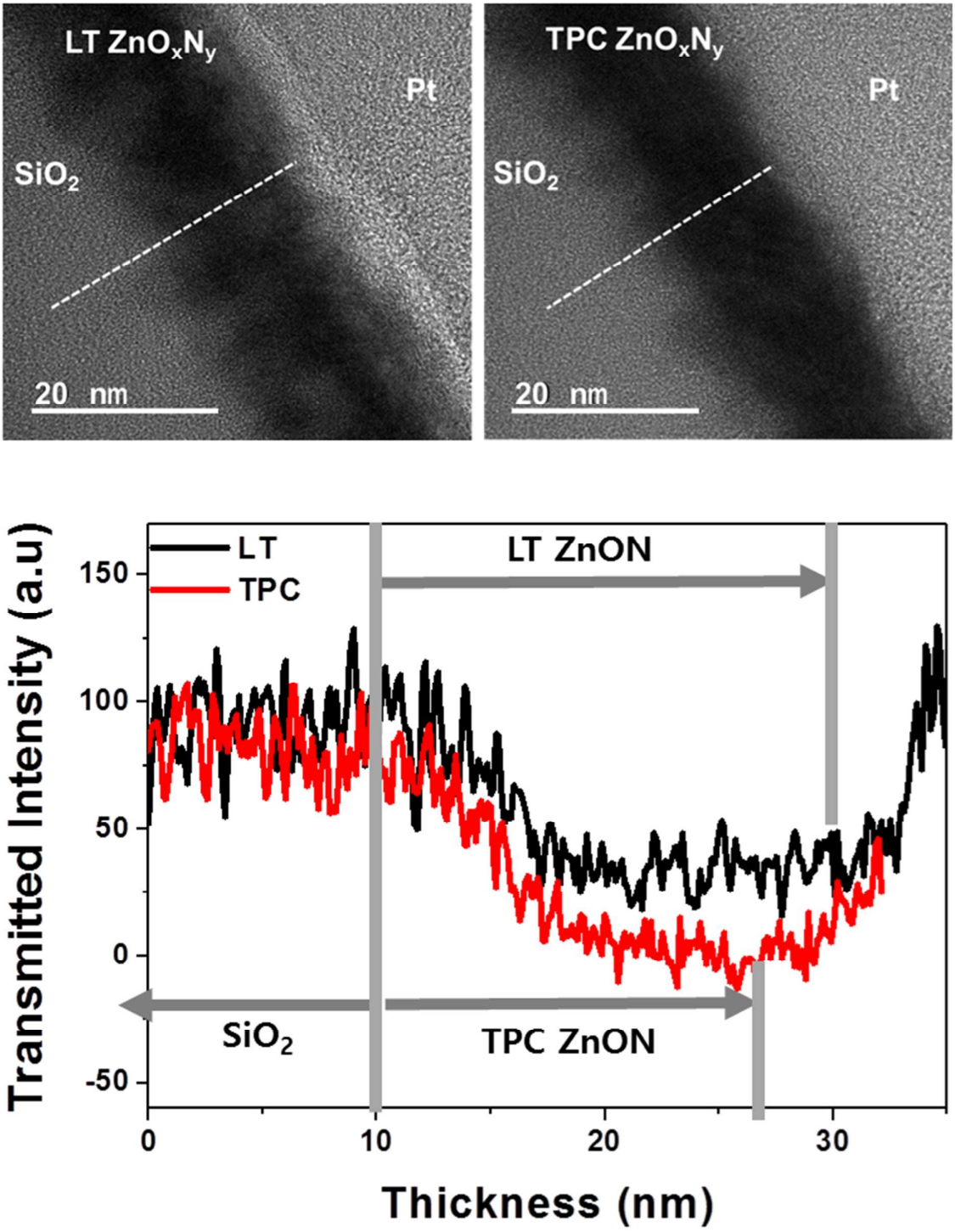

Figure S2. Cross-sectional HR-TEM images of LT- and TPC-treated ZnO_xN_y films and the profiles of transmission electron intensity of the films.

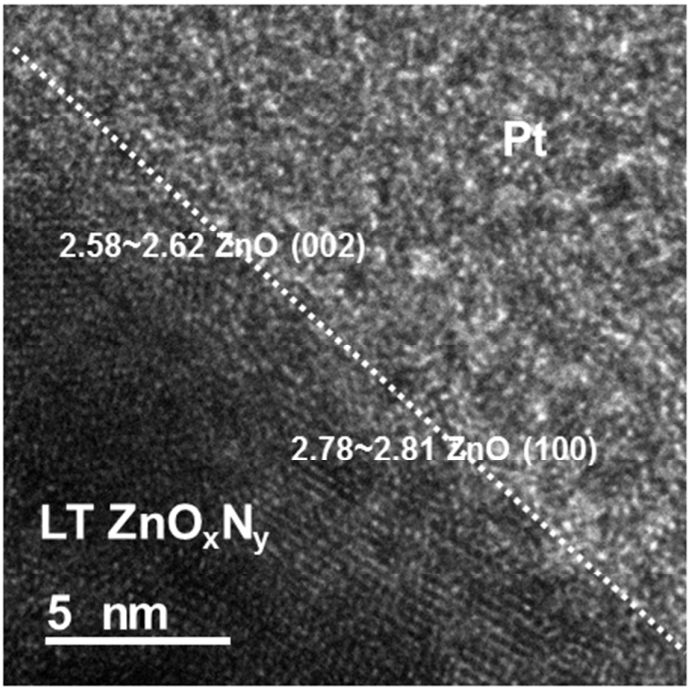

Figure S3. Cross-sectional HR-TEM image of the LT-treated ZnO_xN_y film; nanocrystalline ZnO phase oriented with (002) and (100) on the upper side.

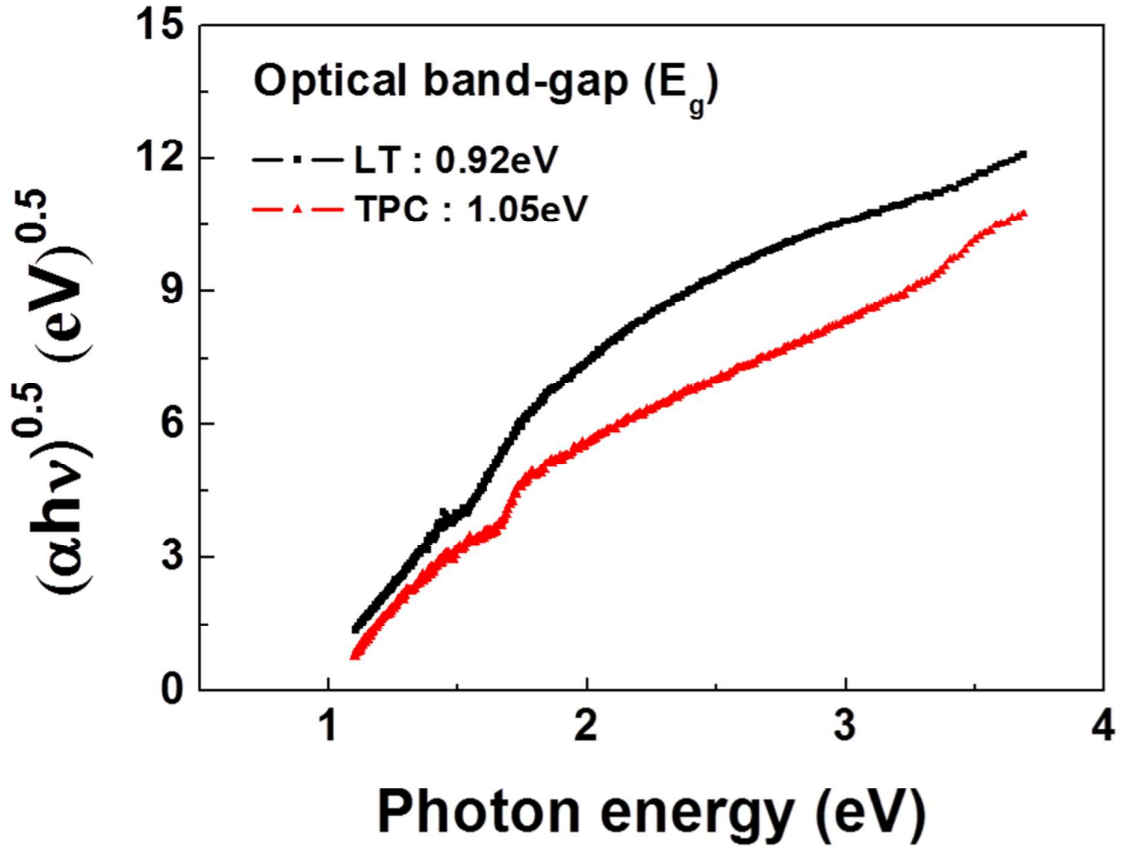

Figure S4. Optical band gap (E_g) of LT- and TPC-treated ZnO_xN_y films.